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Nold et al.

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[54] FURNACE CONTROL APPARATUS AND METHOD

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[57] ABSTRACT

[21] Appl. No.: 886,275

An electric control for gas furnaces which controls a two speed main blower fan and an induction draft fan based on inputs from a room thermostat, a high limit and an ignition control including a gas valve. The control has a circuit board having a power supply for providing 24 volts DC current source to drive DC relays and a 5 volt DC power source to power a microprocessor. 24 volt AC input signals are coupled to the input ports of the microprocessor through current limiting resistors and to AC ground through pull down resistors. AC ground is also connected to the IRQ port of the microprocessor. The output ports of the microprocessor are connected to a relay driver which in turn is connected to the relays. Several breakaway tabs in the board provide optional features such as eliminating a normally provided draft delay timing function. Test pads are provided on the board so that the board can be tested during manufacture. An optional feature is shown comprising an LED which can be used to indicate the status of the system. Another optional feature incorporates a zener diode and resistor coupled to each input port to increase input thresholds. This feature is provided for use with power stealing electronic thermostats.

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[51] Int. Cl.⁵ G05B 13/02; F24H 3/00; G05D 29/00

[52] U.S. Cl. 318/672; 318/62; 318/102; 318/459; 318/471; 318/567; 388/907; 388/934

[58] Field of Search 318/567, 34, 268, 471, 318/472, 51, 53, 59, 62, 66, 67, 101, 102, 103, 443, 445, 484, 668, 671, 672, 634, 641; 388/934, 907.5; 307/38, 39, 40, 41, 115

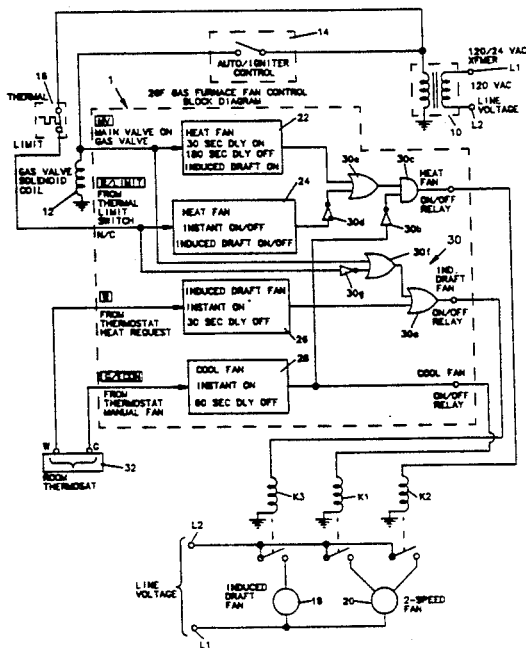
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The control calibrates itself on a continuing periodic basis to read the AC inputs synchronously at the peak of their wave and switches the relays asynchronously based on the real time clock of the microprocessor.

22 Claims, 18 Drawing Sheets



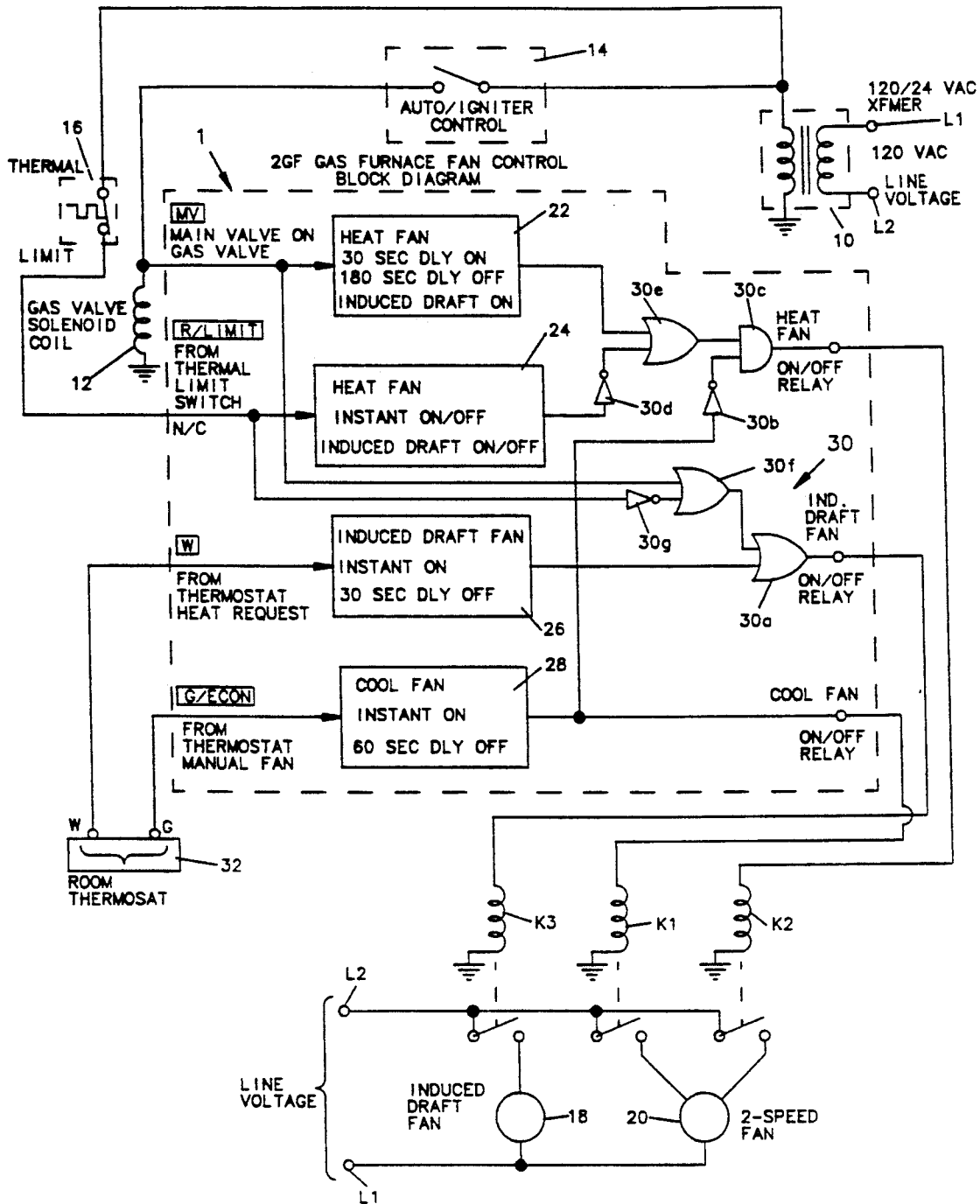


Fig. 1.

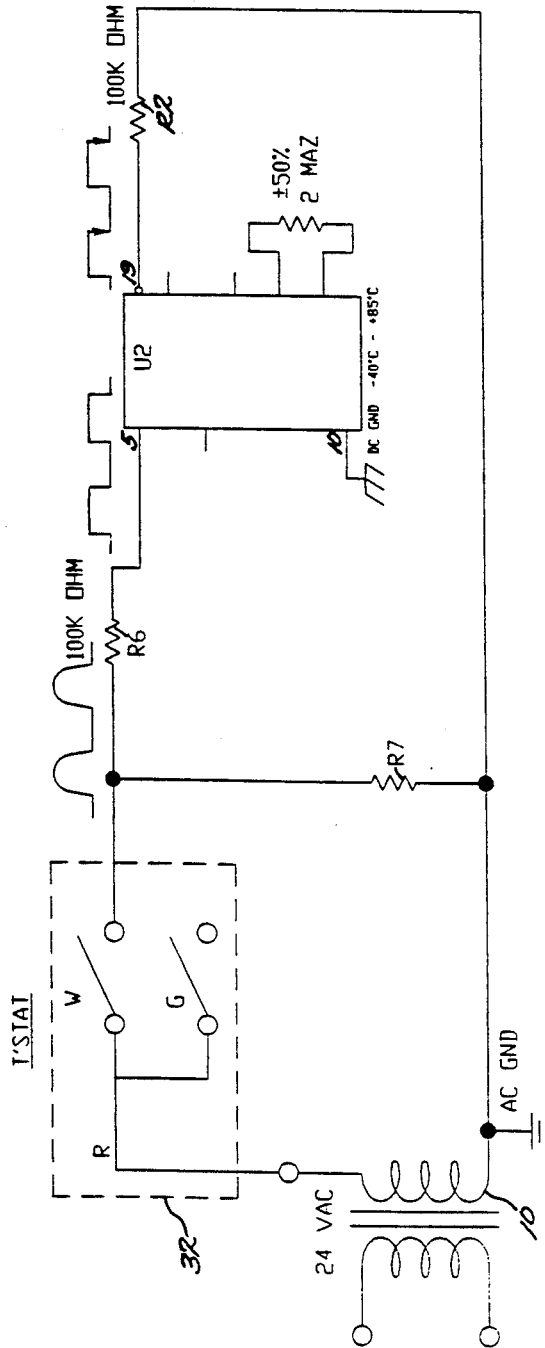


Fig. 3.

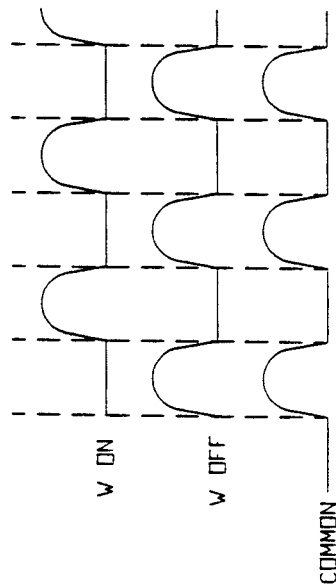


Fig. 3a.

THIS ROUTINE EXECUTED
60 TIMES / SECOND (LINE FREQ)

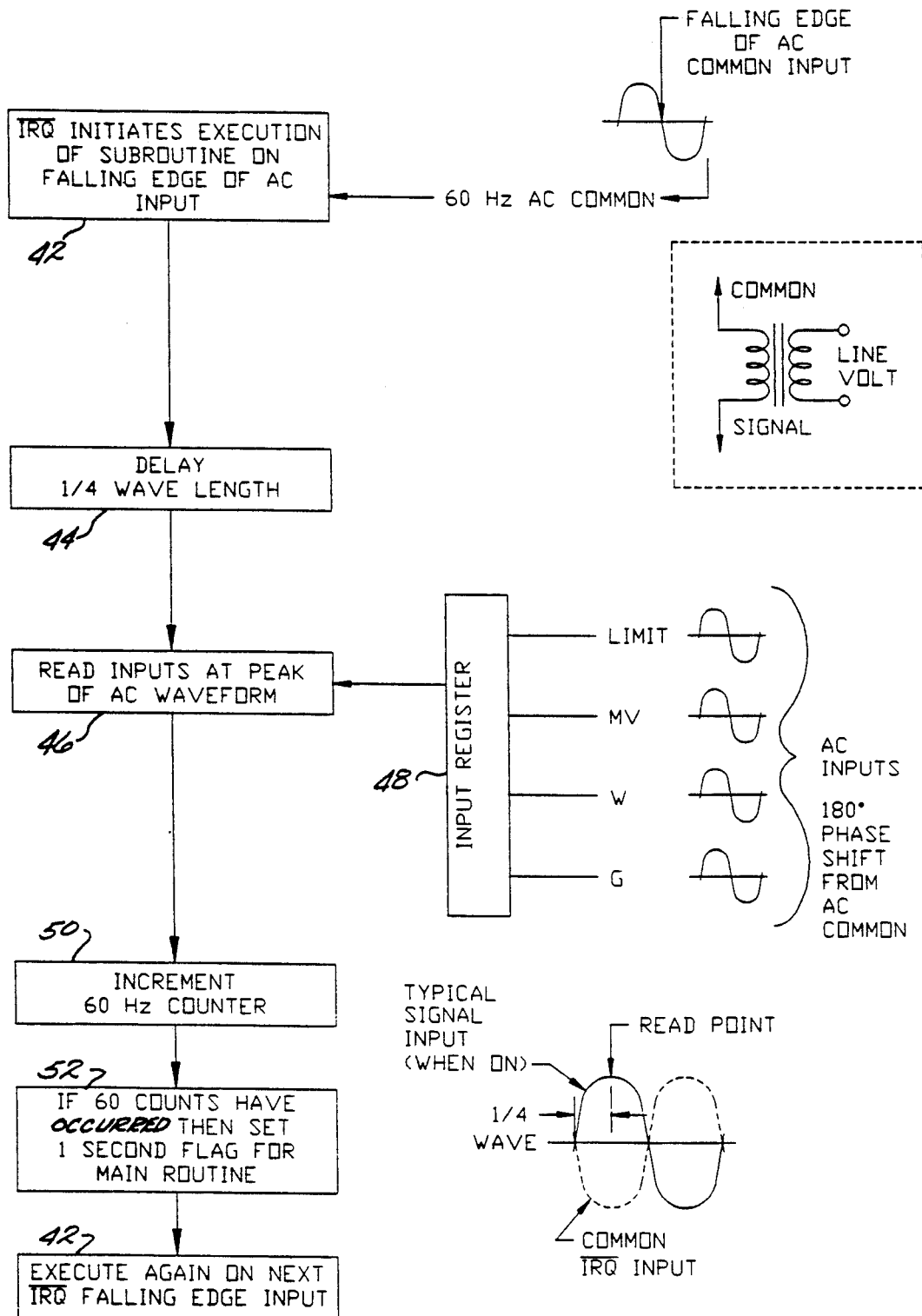


Fig. 4.

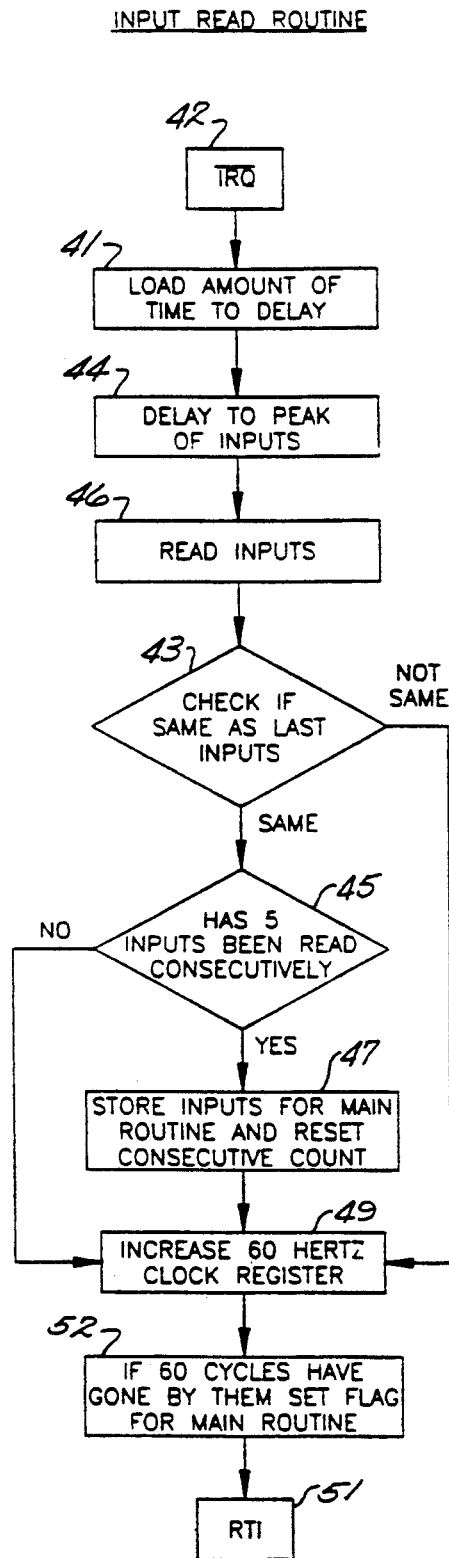


Fig. 5.

INPUT CALIBRATION ROUTINE

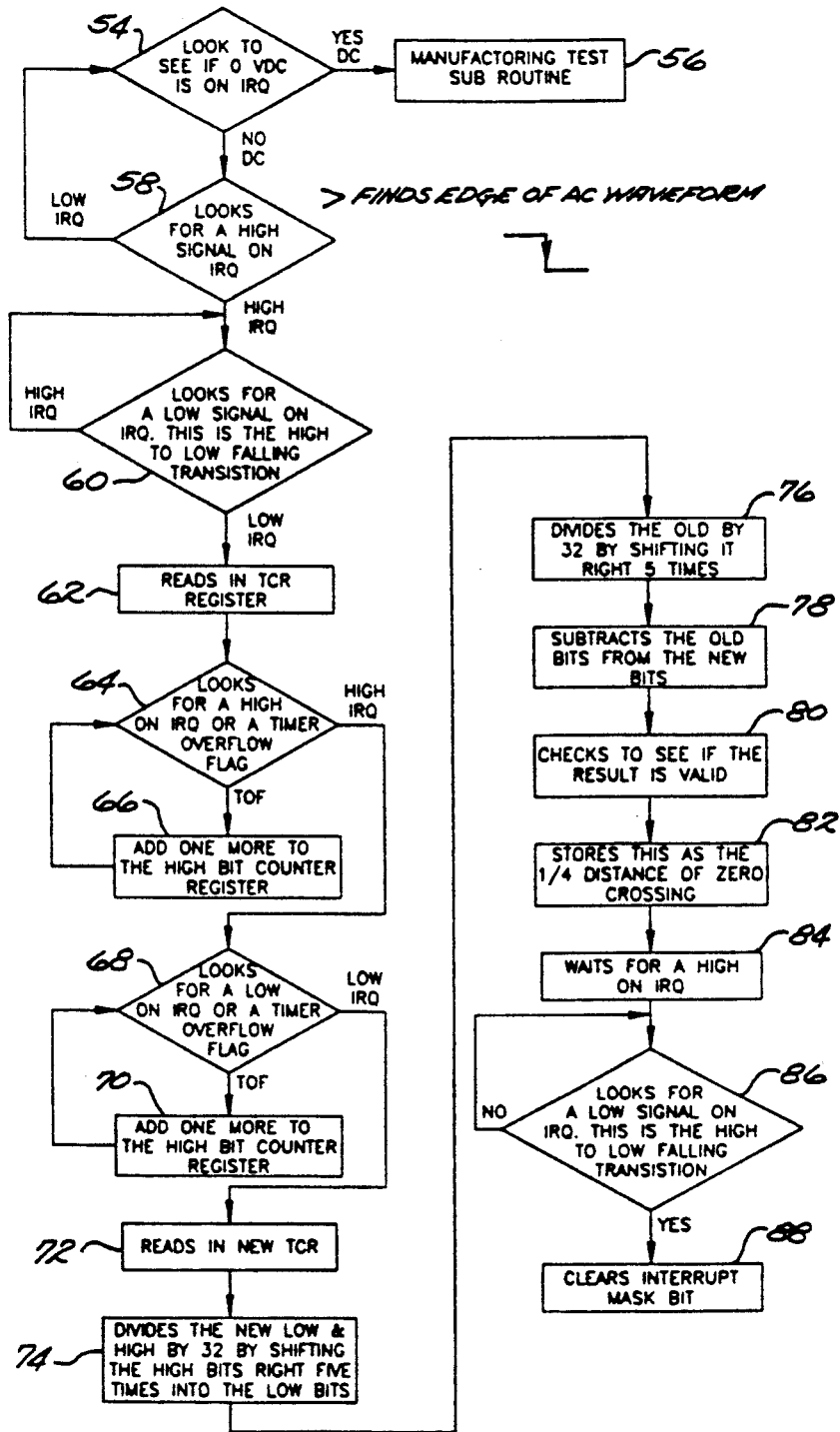


Fig. 6.

PROGRAM OVERVIEW

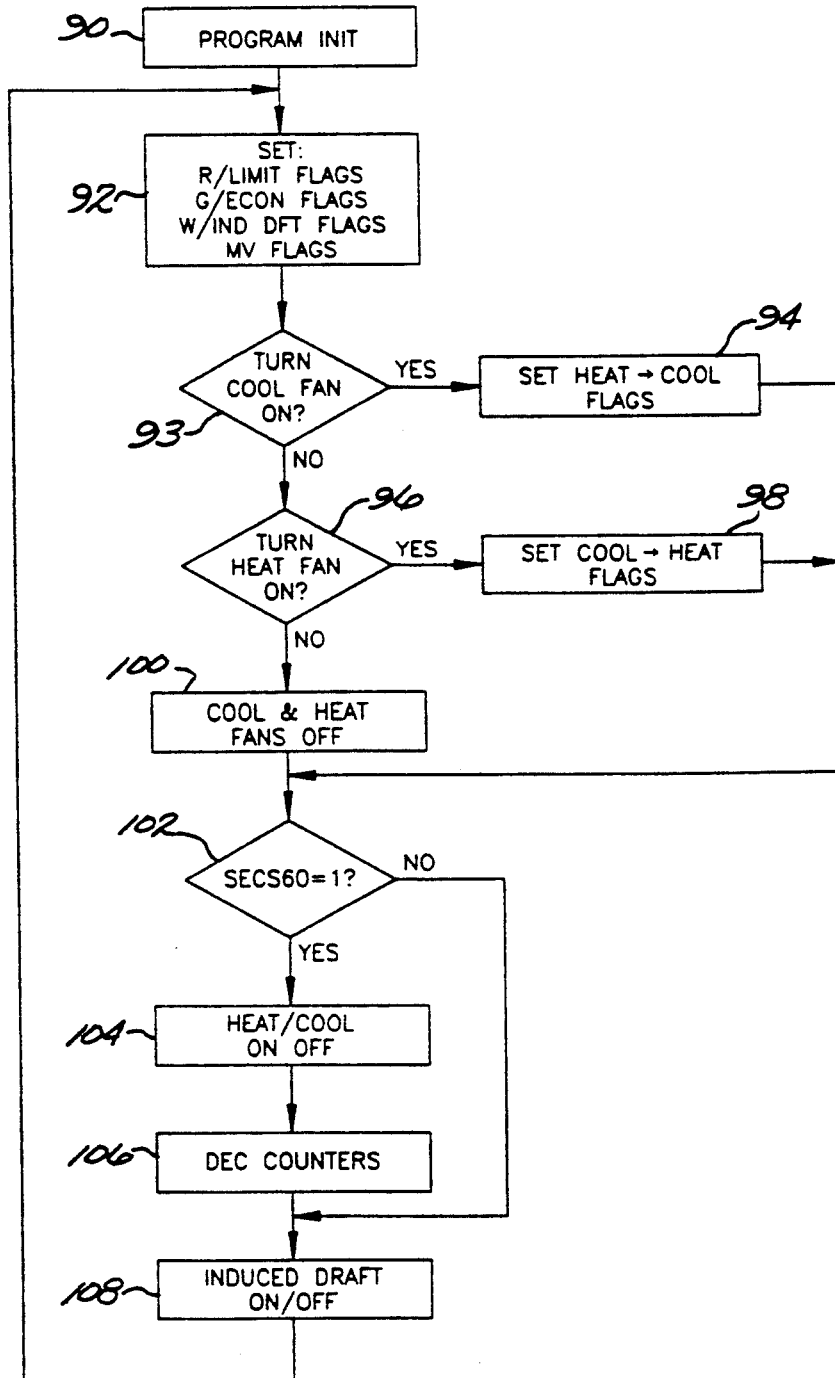


Fig. 7.

FLAG ROUTINE
FOR R/LIMIT, GECON, W/IND DFT

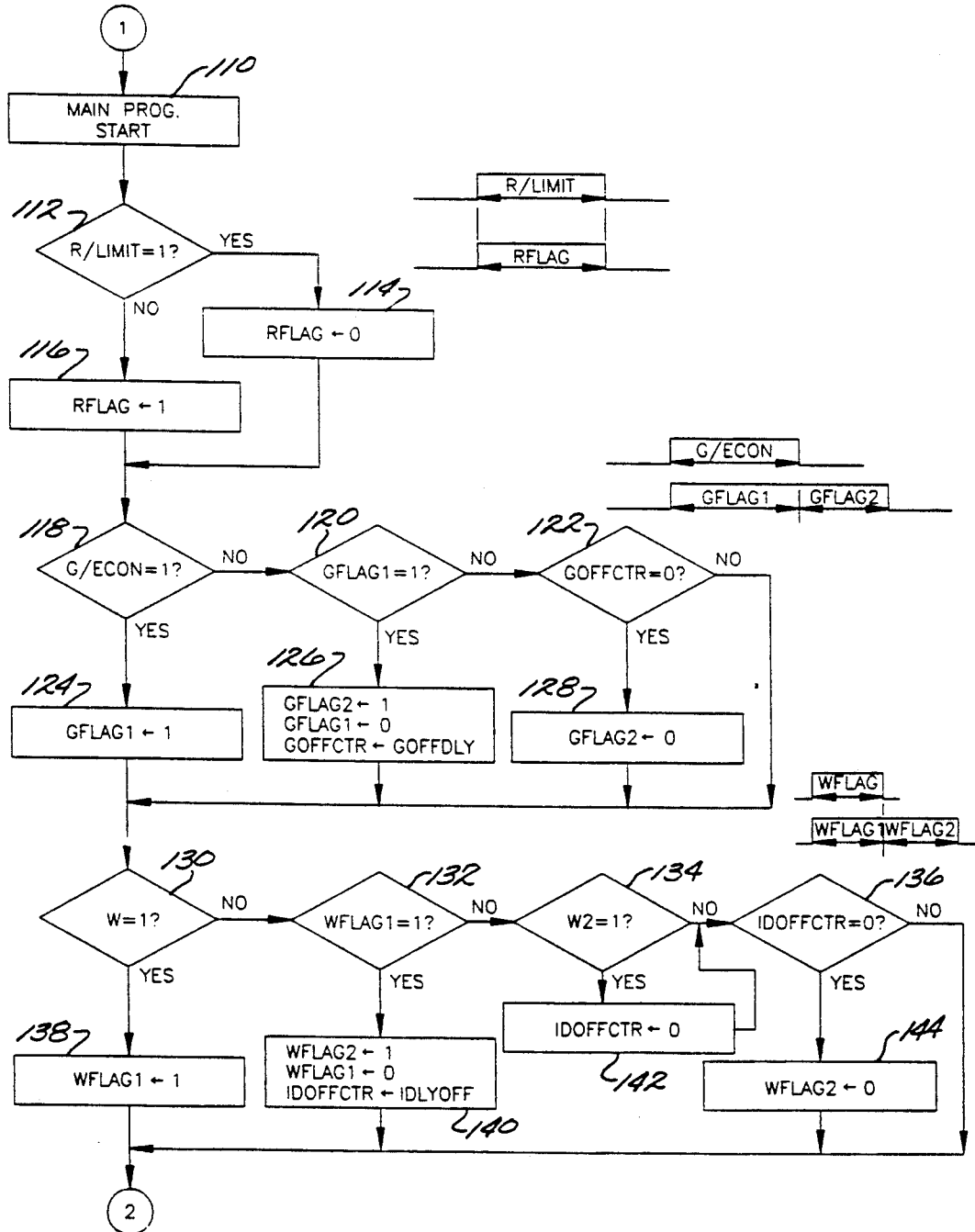


Fig. 8.

FLAG ROUTINE
FOR MV

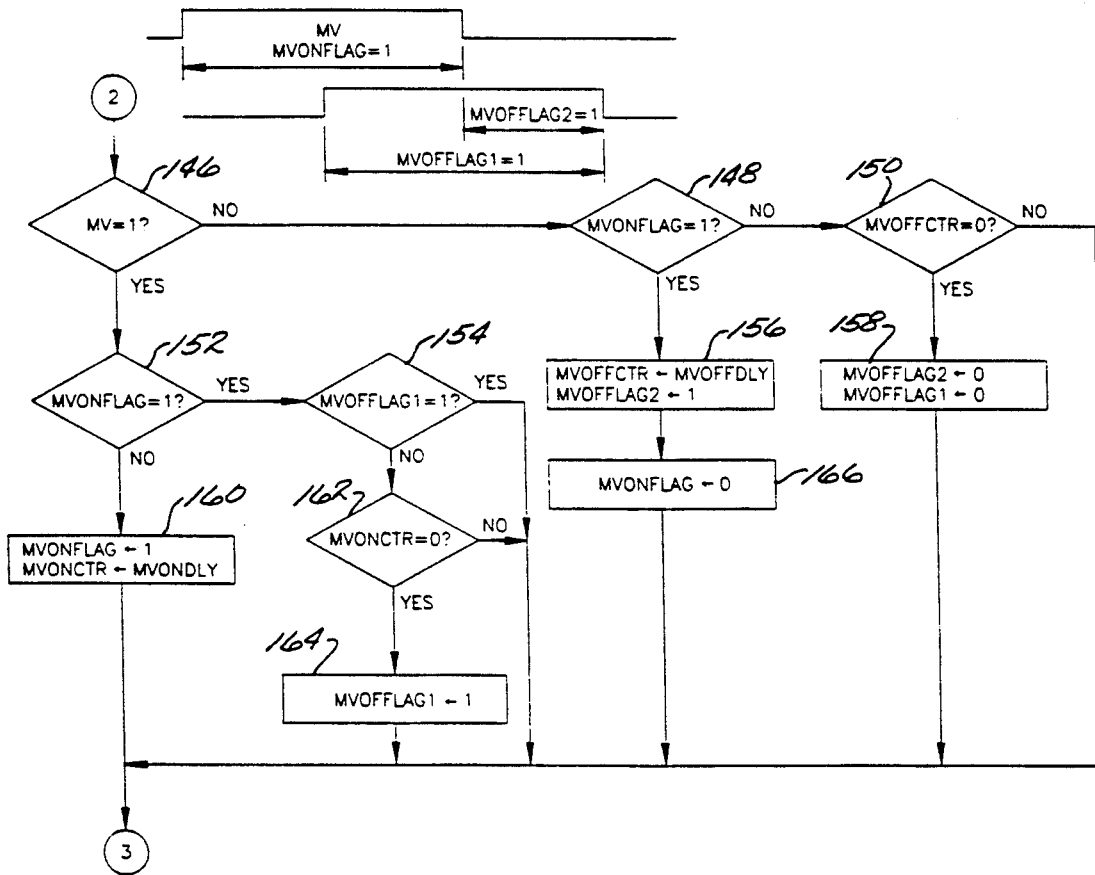


Fig. 9.

OUTPUT FLAG ROUTINE

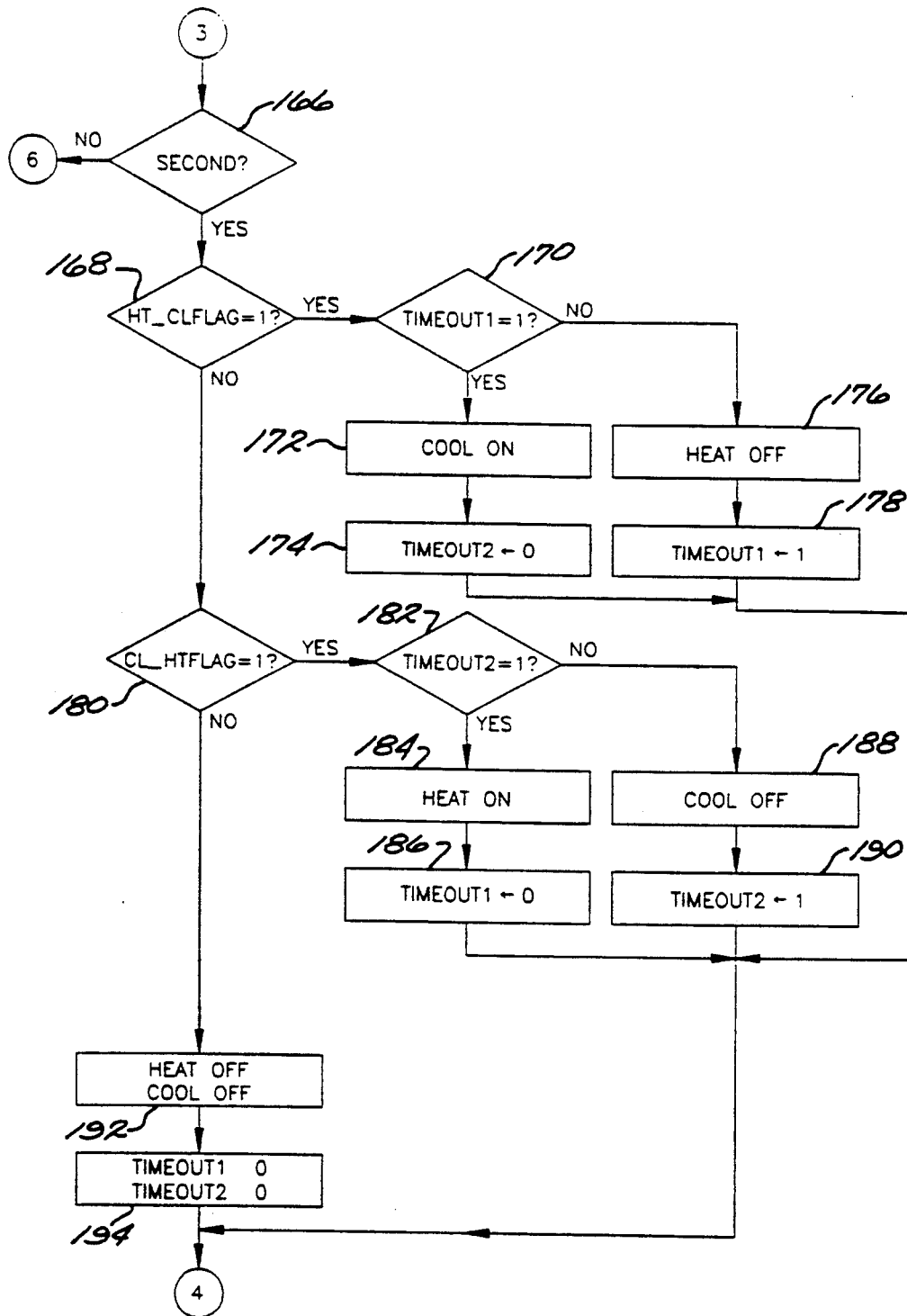


Fig. 10.

OUTPUT ROUTINE

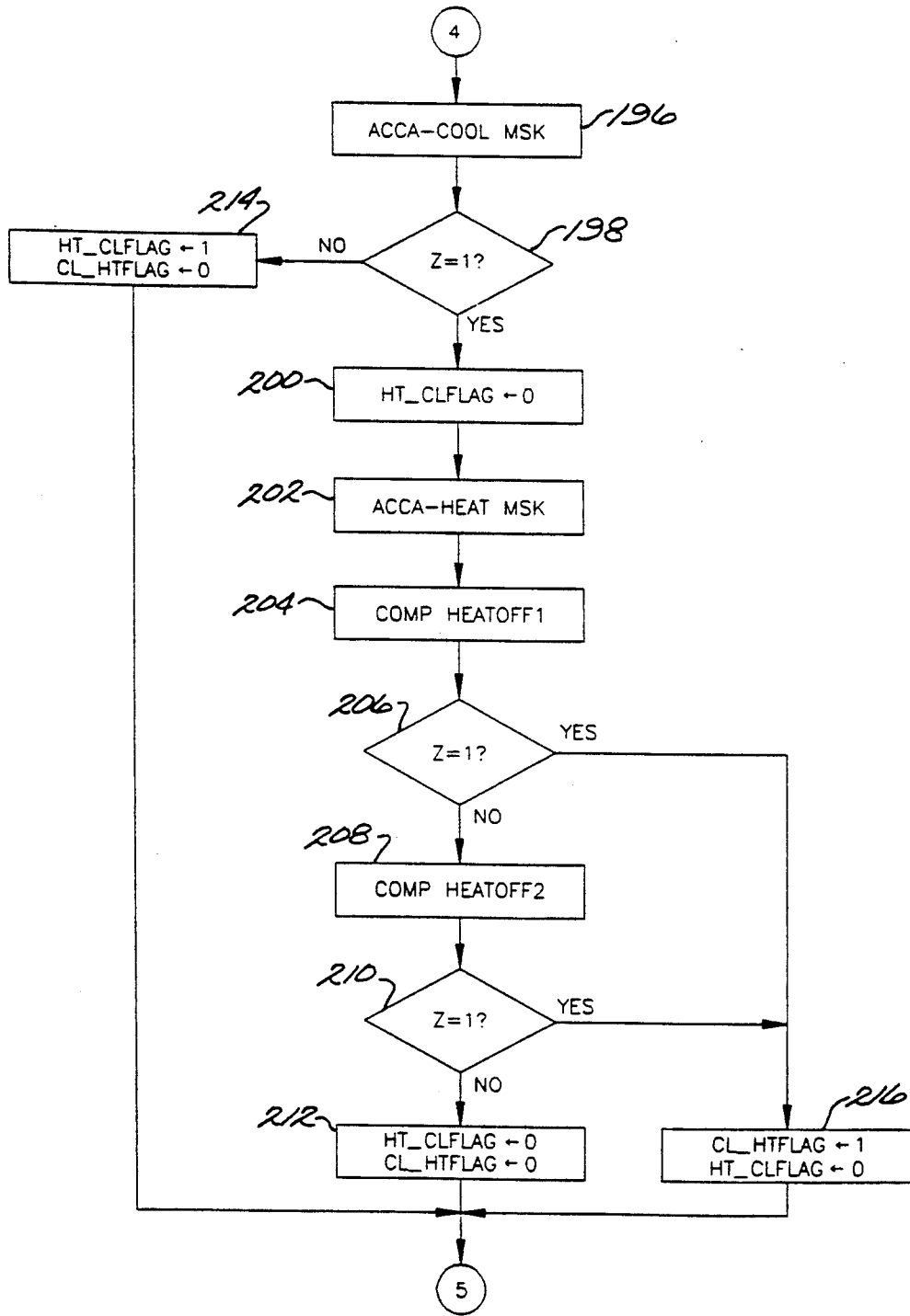


Fig. 11.

COUNTER ROUTINE

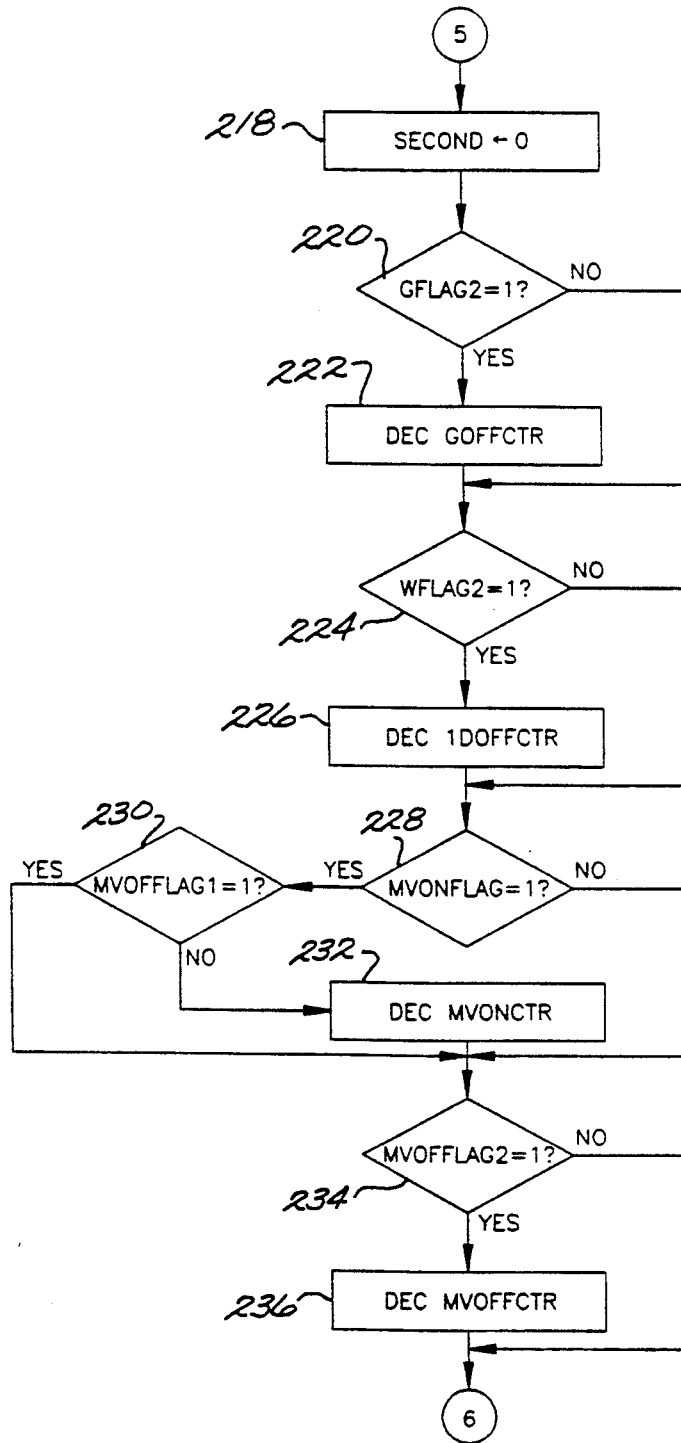


Fig. 12.

INDUCED DRAFT OUTPUT ROUTINE

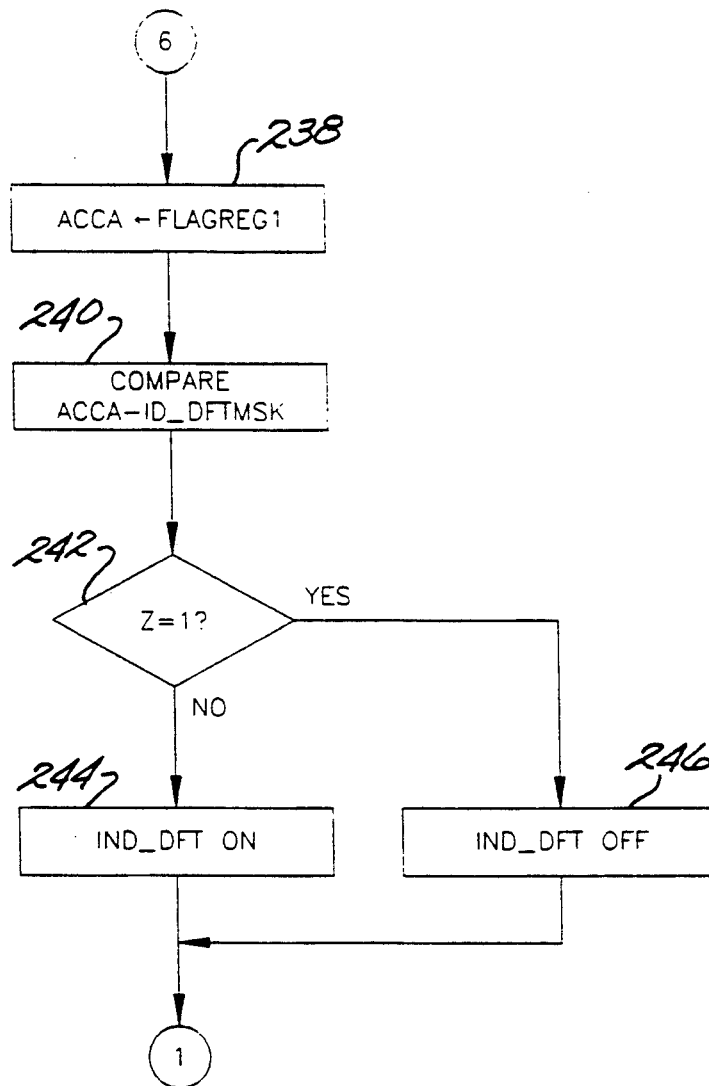


Fig.13.

MEMORY MAP

COUNTERS

G OFFCTR
 I DOFFCTR
 M V OFFCTR
 M V OFFCTR

FLAGS

G FLAG1, G FLAG2
 W FLAG1, W FLAG2
 M V ON FLAG
 M V OFF FLAG1, M V OFF FLAG2

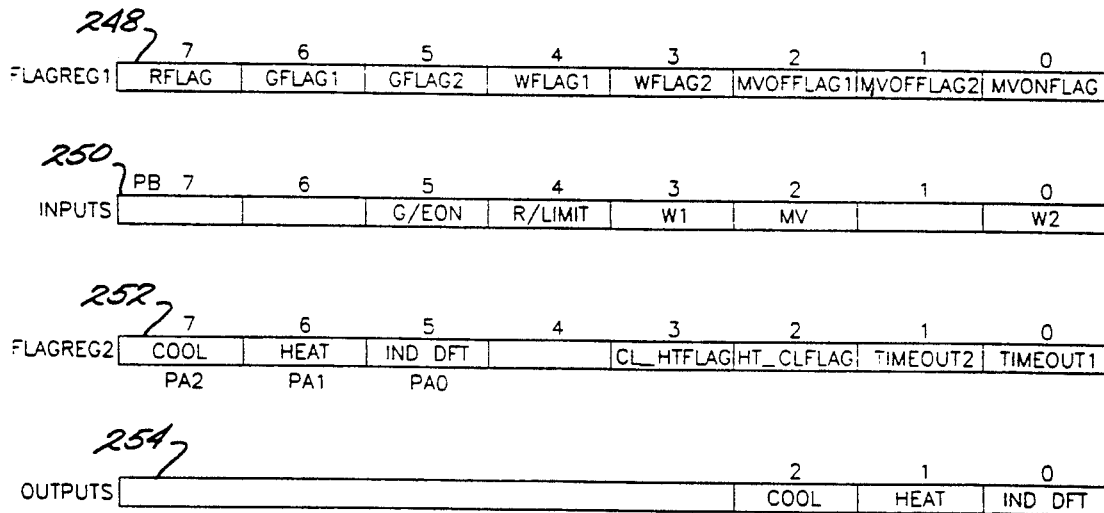


Fig. 14.

HEAT TRUTH TABLE

INPUTS				OUTPUT
RFLAG	MVONFLAG	MVOFFLAG1	MVOFFLAG2	HEAT
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Fig. 15.

COOL TRUTH TABLE

INPUTS		OUTPUT
G/ECON	GDLYOFF	COOL
0	0	0
0	1	1
1	0	1
1	1	1

Fig. 16.

INDUCED DRAFT TRUTH TABLE

INPUTS				OUTPUT
RFLAG	MVONFLAG	WFLAG1	WFLAG2	IND DFT ON
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Fig. 17.

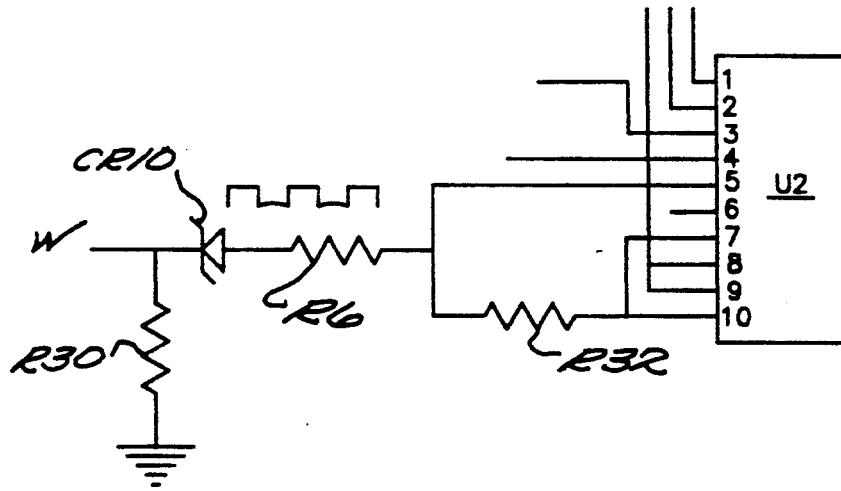


Fig.18.

FURNACE CONTROL APPARATUS AND METHOD

BACKGROUND OF THE INVENTION

This invention relates generally to furnace controls and more specifically to microprocessor based gas furnace controls.

Typically, the control of gas furnaces includes the control of main and induced draft fan motors having selected time delays in conjunction with an ignition control, gas valve and thermostat.

Control of these functions by a microprocessor is known; however, such controls have suffered from the limitation that their timing mechanisms have been more erratic than desirable. Utilizing IC networks such as internal oscillator for timing results in an unsatisfactory tolerance with timing varying plus or minus fifty percent or more. Not only does the timing vary within a particular microprocessor but also from one microprocessor to another. There is a need to provide a control which has significantly improved reliability, particularly in relations to providing consistent timing functions over a wide temperature range, e.g., from minus 40° C. To 85° C.

It is an object of the present invention to provide a control for gas furnace controls which has improved, consistent and reliable timing.

Another object is the provision of a microprocessor control which has timing consistency within plus or minus ten percent over a temperature range of minus 40° C. to 85° C.

Yet another object of the invention is the provision of a microprocessor furnace control which is of relatively low cost, reliable and one which results in improved relay contact life.

BRIEF SUMMARY OF THE INVENTION

Briefly, in accordance with the invention, a control circuit controls the heat speed and cool speed of a fan motor based on inputs from a room thermostat, a gas valve and a high limit switch. All the control inputs are 24 VAC signals which are inputted to a microprocessor through current limiting resistors and with the IRQ input connected to the 24 VAC transformer common which, according to a feature of the invention, is used to provide a reference point for reading the input signals. The microprocessor outputs directly drive a relay driver in the form of an array of darlington transistors which operate DC relays. The control circuit has a power circuit providing 24 VAC and a full wave rectified voltage to power the relays as well as 5 VDC required of the microprocessor.

According to a feature of the invention a calibration routine is executed upon initialization and on an ongoing basis to synchronize readings of the AC inputs. The input routine executes as an IRQ interrupt routine and reads the inputs at the peak of the AC signal and must read a selected number of good readings before updating an input register. A one second flag is also derived from this 60 hertz input routine.

According to another feature of the invention the output is executed based on the Real Time Interrupt Clock which operates from the internal oscillator which is asynchronous to the 60 hertz line frequency. The output port is updated with the contents of the output register on every interrupt.

According to another feature of the invention the main control program causes the inputs to be read and flags set for the present and previous states and based on the status of the flag registers the output register is updated. Timing functions are performed using the one second clock and counting registers. The program verifies that the interrupt routines are working before executing the main program. If an interrupt does not occur within the watchdog period the microprocessor is reset. When the outputs are idle the microprocessor generates an internal reset every 256 seconds.

According to a feature of the invention when the IRQ line is at DC a test sequence occurs on the inputs with the part number, revision number and status outputted. The microprocessor can be put into an accelerated timing mode for further testing.

In a modified embodiment particularly adapted for use with electronic thermostats a selected pull down resistor is connected to the input signal lines along with a zener diode. This results in increased switching threshold voltages from the thermostat and allows compatibility with power stealing thermostats.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic of a system in which a circuit board made in accordance with the invention is used with the board shown by functions performed by the control;

FIG. 2 is a schematic of the FIG. 1 system in which the structural components of the circuit board is shown; FIG. 2a shows the component layout on the circuit board along connections to the several system components;

FIG. 3 is a simplified version of FIG. 2 showing one of the AC input signal lines and the microprocessor and several wave forms;

FIG. 3a depicts wave forms relating to FIG. 3;

FIG. 4 shows key steps of an input reading routine used in accordance with the invention along with explanatory material inter-relating signal and common wave forms;

FIG. 5 is the input read routine of FIG. 4;

FIG. 6 is an input calibration routine used in accordance with the invention;

FIG. 7 is a main program overview; FIG. 8 is a flag routine for R/LIMIT, GECON; W/IND DFT;

FIG. 9 is a flag routine for MV (main valve);

FIG. 10 is an output flag routine;

FIG. 11 is an output routine;

FIG. 12 is a counter routine;

FIG. 13 is an induced draft output routine;

FIG. 14 is a memory map;

FIGS. 15-17 are truth tables for heat and cool speeds and induced draft fans respectively; and

FIG. 18 shows a portion of the FIG. 2 schematic modified to provide electronic thermostat compatibility.

DETAILED DESCRIPTION OF THE DRAWINGS

With particular reference to FIG. 1 the several components of the system are shown along with a schematic representation of the functions provided by the control made in accordance with the invention.

A 120/24 VAC transformer 10 provides 24 volt AC power to a gas valve solenoid coil 12 and MV terminal on control board 1 through autoigniter control 14. The

24 volt AC power is also connected through a thermal limit 16 to R/Limit terminal on control board 1. Terminals W and G of a room thermostat 32 are connected respectively to terminals W and G/ECON on board 1.

An induced draft fan motor 18 and a two speed fan motor 20 are shown connected across line voltage L1, L2. Energization of fan motor 18 is controlled by a relay coil K3 from an output on board 1 and energization of cool speed and heat speed of fan motor 20 are controlled respectively from outputs on board 1 by relay coils K1 and K2.

Control board 1 is shown with functional blocks 22, 24, 26 and 28. Block 22, which receives an input from terminal MV, main valve, provides a heat fan energization signal with a selected time delay of 30 seconds on and 180 seconds off and an instantaneous induced draft fan energization. Block 24, which receives an input through normally closed thermal limit switch 16, provides a heat fan energization signal, instant on and off and induced draft fan energization, instant on and off. Block 26, which receives a heat request input from terminal W of room thermostat 32, provides an induced draft fan energization signal, instant on and a thirty second delay off. Block 28, which received a manual cool fan request input from room thermostat 32, provides a cool fan motor energization signal, instant on and a sixty second delay off.

Also shown in FIG. 1 are a group of symbols 30 used to describe the logic inter-relating the various inputs to provide the desired functional outputs which are actually provided in the software routines to be discussed below.

Thus a G signal received from room thermostat 32 turns on the cool fan instantly which remains on for sixty seconds after the signal is turned off at the room thermostat. A W or a heat request signal from the room thermostat is shown going through an OR gate 30a results in the induced draft fan being turned on instantly and remaining on for thirty seconds after the W signal is turned off at the thermostat.

A G input is also shown connected through an inverter 30b to an AND gate 30c whose output is connected to the heat fan coil K2 so that an on or high signal from block 28 will be converted to a low signal being input to AND gate 30c indicating that a cool speed fan request will override a heat speed fan request.

Thermal limit switch 16 is normally always energized providing a high input to block 24, which is inverted to a low through inverter 30d, and a normal low input to OR gate 30e. When autoigniter control 14 is energized a high will be input to block 22 which will result in a high output from OR gate 30e and, assuming a low cool fan signal, will result in a high from AND gate 30c thereby energizing heat from relay coil K2. Energization of the gas valve 12 also provides a high input into OR gate 30f which in turn provides a high input to OR gate 30a to energize induced draft fan relay coil K3.

If thermal limit switch 16 opens because of a fault condition it provides a low input to inverter 30g which results in a high input to OR gate 30f thereby providing a high input to OR gate 30a and energization of induced draft fan 18. In addition, unless there is a signal calling for cool fan energization then the opening of thermal limit 16 will cause energization of heat fan relay coil K2 by providing a low input to inverter 30d which is changed to high input to OR gate 30e and a high input to AND gate 30c.

Turning now to FIG. 2 a schematic representation is shown of a control circuit made in accordance with the invention along with other components of a gas furnace system with which the control circuit is used. Transformer 10, providing 24 volts AC from line voltage, is connected at the 24 VAC output side to connector Q11 and then through a 5 amp fuse F1 to a full wave bridge comprising diodes CR1, CR1, CR3 and CR4. The transformer common is connected to the bridge through connector Q12. The bridge provides full wave rectified 24 VAC power to drive relays K1, K2 and K3 to be discussed below. Zener diode CR7 suppresses back EMF. Capacitor C2, resistor R15 and capacitor C1, resistor R1 provide 5 volts DC on line VDD for the power supply of microprocessor U2 to be discussed below.

There are several low voltage AC input terminals labeled Y1, Y2, C, G, R, W1, W2 and ECON. Terminals Y1, Y2 are not used in the present embodiment. Terminal C is connected to the transformer common, terminal G is coupled to an output of room thermostat 32 and to input port 3 of microprocessor U2 through a 100K ohm resistor R3 and is connected to common through pull down resistors R12, R13, R14 of 1.5 ohms connected in parallel to provide an equivalent resistance of 500 ohms. Terminal G is also connected to the terminal ECON. A signal on the G terminal results in energizing the manual fan as well as providing a cool request as will be explained further below. Terminal W is coupled to an output of room thermostat 32 and to the ignition control module 14, the other side of which is connected to common through the gas valve solenoid coil 12 and to connector Q14. Terminal W1, interconnected with terminal W2, is connected to input port 5 of microprocessor U2 through limiting resistor R6 of 100K ohms and to common through pull down resistor R7 of 50K ohms. Connector Q14 is connected to the 24 VAC output of transformer 10 through 100K ohm pull up resistor R9 and to input port 6 of microprocessor U2 through limiting resistor R8 of 100K ohms. It should be noted that there is no separate pull down resistor required since the main valve itself serves as a pull down resistor. Pull up resistor R9 serves as a safety feature. That is, if for any reason, the gas valve is not correctly wired to the control circuit since there is no pull down resistor to common pull up resistor R9 will always provide a high input thereby turning the induced draft fan on.

Another input to microprocessor U2 is IRQ port 19 which is a common input received through 100K ohm resistor R2. Clamping diode CR6 connected between port 19 and the 5 volt supply VDD drops the input at 5 volts.

Microprocessor U2 has two additional, optional inputs provided by breakaway tabs 34, 36. Input port 15 is connected to the 5 volt supply VDD through breakaway tab 36 and to DC ground or common VSS through 10K ohm resistor R10. Normally the system provides a selected period of time that the draft fan is maintained in the energization condition after its energization signal has been removed. This occurs when port 15 is pulled high by its connection with the 5 volt supply VDD. However, if tab 36 is broken off resistor R10 will pull port 15 to ground providing a low. Then the draft fan is turned off at the same time its energization signal has been removed.

Similarly, port 17 is connected to the 5 volt supply VDD through tab 34 and to ground VSS through 10K ohm resistor R17. Tab 34 provides a pilot draft option.

Reference numeral 38 indicates a wiring point which is used for testing the control. That is, by placing a 5 volt DC input at point 38 the control is placed in a test mode in effect shortening all the normal time delays. Point 38 is connected to port 16 of microprocessor U2 and ground through 10K ohm resistor R16. DC ground VSS is also connected to ports 10 and 7 of microprocessor U2.

Output ports 11-14 are connected to relay driver integrated circuit U1 at pins 7, 6, 5 and 4 respectively. Relay driver U1 comprises a transistor network which, in effect, switch on relays K1, K2, K3 when the base of the transistors receive an input signal from microprocessor U2. Output pin 12 of relay driver U1 is connected to the coil of relay K3 which has a common contact connected to power connectors Q16, Q17 and a normally open contact connected to connector Q25.

Power connectors Q16, Q17 are connected to switching mechanisms in respective relays K1, K2, K3. Energization of the relay coil of relay K1 through output port 11 will cause the switch to connect power to terminal Q21, the cool speed of the fan motor. Energization of the relay coil of relay K2 through output port 13 will cause the switch to connect power to terminal Q22, the heat speed of the fan motor. Energization of the relay coil of relay K3 through output port 12 will cause the switch to connect power to terminal Q25, the induced draft fan motor.

An optional feature is shown at the dashed line box identified by numeral 40 comprising resistor R18 serially connected to LED between pin 10 of relay drive U1 and common, pin 9. This feature provides a flashing or continuous LED based on the state of the inputs.

Resistor R11 of 39K ohms is connected to pins 1 and 2 of microprocessor U2 to provide a selected rate of oscillation for the internal clock.

The control board is provided with Q9 and Q10 to connect the high limit switch. The high limit switch is normally closed but adapted to open upon an over temperature condition. An economizer function is tied to terminal G. This can be used as an output in a system having an economizer, i.e., an option which, for example, opens a duct to outside fresh air when the manual fan is on.

With reference to FIG. 3 which is a simplified portion of FIG. 2, one of the inputs will be described. With respect to the W terminal, due to the internal structure of the CMOS microprocessor which includes intrinsic diodes on both the P and N channels of the FETs which serve to limit input voltage to 5 volts, a simple current limiting resistor R6 can be inputted to port 5 of microprocessor U2 along with a resistor R7 tied to common. When the room thermostat 32 provides a heat request signal by connecting 24 VAC from transformer 10 a wave form on the W line is shown in FIG. 3a as W_{on} . When terminal W is not energized port 5 of the microprocessor is tied to common with its wave form shown at W_{off} , which is the same as common.

The 5 volt DC ground coming from the diode bridge is shown at port 10. With respect to DC ground the microprocessor sees a half wave which, because of the diode clamping is a square wave having the line frequency of 60 HZ, the phase of which depends on whether the W terminal is closed or open. When the terminal is closed the wave is 180° out of phase with the

common voltage but when the terminal is open it is in phase with common voltage. In effect when the thermostat calls for heat a connection is made with the high side of the transformer, 180 degrees out of phase with common, and when it does not call for heat the connection is with the common of the transformer. AC common is connected to port 19, the IRQ or special interrupt port of microprocessor U2 through resistor R2. As indicated in FIG. 4, at the block, 42 the IRQ initiates execution of a subroutine whenever it is exposed to the falling edge of an AC input. Thus that routine is directly tied to common and is executed on every falling edge of the square wave. According to the routine, block 44, there is a delay of a quarter of a wave length and then the input port, in this case port 5, block 46, is read and inputted to the input register 48 for use in the main routine and a 60 HZ counter is incremented, block 50. After sixty counts, block 52, (i.e., one second) a flag is set so that the timing information can be transferred to the main routine. Thus the subroutine is executed with the input register 48 updated on every falling edge of the 60 HZ wave.

The specific delay of a quarter of a wave length is determined by the relationship between the microprocessor clock and the AC clock or frequency. At the beginning of the main routine while the interrupt is masked a subroutine reads the real time clock counter, then when the edge of the wave at port 19 goes high, an active low, the real time clock is read. When the IRQ goes low again (one cycle of the 60 HZ later) the real time clock is read again so that the number of clock pulses the oscillator has gone through during this cycle can be determined. The oscillator runs much faster, for example, in the order of 2 megahertz. The result, which varies from chip to chip, is used to synchronize the real time clock and the line clock and derive how many oscillations are in a quarter cycle. Once this calibration routine is accomplished a clear interrupt is generated so that the IRQ input is enabled to start working in the main program reading the input signals at the high point of the signal wave.

The relays are actuated asynchronously in order to have the contacts close randomly with respect to the AC line wave so that the load is more evenly distributed on the contacts. That is effected by using the real time or internal clock. A real time interrupt which counts directly from the oscillations at the real time clock sets a real time interrupt flag (RTIF) thereby generating an internal interrupt to execute a subroutine used for the output. When the real time interrupt flag is set the output section of the code is executed resulting in the asynchronous switching of the relay contacts.

With respect to the specific routines, FIG. 5 shows the input read routine wherein the inputs are checked in relation to previous inputs to see if a sufficient number of good inputs have been read and if so a flag is set for the main routine. The routine is initiated at 42 with the time delay to the peak of the input wave at 41, 44 and the input read at 46. A decision block 43 checks to see if the input is the same as the previous inputs and if not the routine goes to processing block 49 which increases the 60 Hertz clock register. If the inputs are the same it moves to decision block 45 to see if 5 inputs have been read consecutively and if not again jumps to processing block 49. If 5 inputs have been read consecutively it goes to 47 storing inputs for the main routine and resets the consecutive count and then goes to block 49 and then, at 51 and 52 sets flag for the main routine.

FIG. 6 shows the flow chart of the input calibration routine in which the IRQ port waits for a low to high transition to find the wave edge which is then read in the TCR register. Since the real time clock has limited capability overflows are counted in order to derive a quarter wave delay time. Essentially the number of internal clock cycles are counted for one AC clock cycle to go by from which the quarter wave delay time is derived. More specifically, the routine includes decision block 54 which checks to see if direct current is on IRQ port and if so goes into the manufacturing test subroutine 56. If not the routine goes to decision block 58 and looks for a high signal on IRQ port. If the signal is low it goes back to decision block 54 while if it is high it moves to decision block 60 where it looks for a high to low falling transition, i.e., a low signal on the IRQ port. If the signal is high it cycles around until it finds a low signal and moves to processing block 62 and reads into the TCR register and goes to decision block 64 where it looks for a high on IRQ port or a timer overflow flag. If it finds a timer overflow flag it adds one more to the high bit counter register at block 66 and goes back to decision block 64. If it finds a high on the IRQ port it goes to decision block 68 where it looks for a low on the IRQ port or a time overflow flag. If it finds a timer overflow flag it adds one to the high bit counter register at 70 and then goes back to decision block 68 and if it finds a low on the IRQ port it goes to block 72 and reads in new TCR and then to processing block 74 where it divides the new low and high by shifting the high bits right five times into the low bits and then to block 76 where it divides the old by 32 by shifting it right five times and in block 78 subtracts the old bits from the new bits and at processing block 80 checks to see if the result is valid and at block 82 stores this result as the one quarter distance from zero crossing and then, at block 84, waits for a high on the IRQ port. The routine then goes to decision block 86 and waits for a low signal, the high to low falling transition, on the IRQ port and then at 88 clears interrupt mask bit.

FIG. 7 shows a simplified overview of the main program which assumes that everything is functioning as intended, i.e., the RTC (clock) is running, the interrupt routines are executing, etc. As the routine is initiated at 90 it takes the inputs and sets condition flags at 92. Then a decision is made at 93 whether the cool fan needs to be on and if so a flag is set at 94 to make the heat to cool transition. If the cool fan is not called for a decision is made at 96 regarding the turning on of the heat fan. If yes, the cool to heat transition flag is set at 98. If the heat fan is not called for then at 100 both heat and cool fans are off. It should be noted that the transitions are always set to avoid the possibilities that both receive a turn on signal at the same time. The routine then at 102 looks to see if one second has passed and if not goes to block 108. Every second the decrement counter is decremented turning the fans on and off as required at 104 and 106. The induced draft fan can be on at the same time the heat fan is on; therefore, it is not included in the sixty second routine. The flags are continuously checked but the induced fan is not turned on and off every second. If one of the flags is set, for example, a flag is set to change heat to cool, the first time through the routine heat speed receives an instruction to turn off for a second, then the next time through the instructions will be turn on the cool speed. This obviates contradictory signals. Whereas whenever the induced fan receives a signal to turn on it can do so without any delay.

FIG. 8 shows the flag routine 110 for R/LIMIT, GECON and W/IND DFT and FIG. 9 for MV including decision and processing blocks 112-164 wherein the conditions of the limit flags are checked, what conditions they are in and where they have been in order to avoid the possibility of short cycling the routine and that the output routine has to finish completely. This is particularly important when some overlapping occurs, that is, competing signals for heat and cool speed fans. For example, the cool speed has a sixty second off delay and the heat speed a three minute off delay. The several flags keep track of these various conditions.

FIG. 10 relating to the output flag routine and including decision and processing blocks 166-914 ensures that the proper sequence of events occurs. That is, that the heat speed is turned off before the cool speed is turned on and the like.

FIGS. 11 and 12 show the output and counter routines respectively including decision and processing blocks 196-236 in which flags are set to transfer the output register in the RTI interrupt routine. Based on the conditions determined by a flag, e.g., if in time delay off then the counter is decremented, if not the routine skips to the next item.

It will be seen in FIG. 13, relating to the induced draft output routine including processing blocks 238, 240, 244 and 246 and decision block 242, that competing speeds are not factors so that the 1 second flags is not a factor.

FIG. 14 shows the several counters and flags and their location in memory including flag register 1-248, inputs 250, flag register 2-252 and outputs 254 while FIGS. 15, 16 and 17 are truth tables of the inputs and outputs of heat and cool speeds and induced draft fan respectively.

A modified embodiment is shown in FIG. 18 to make the control compatible for use with electronic thermostats. Electronic thermostats conventionally use one of the live thermostat lines as common and as long as the outputs have low impedance this does not cause a problem; however, when used with electronics of the type employed in the instant invention the two milliamperes or so of current can cause unintended operation, particularly in the heat request signal line in which the conventional time delay relays have been obviated by the circuit made in accordance with the invention. One way of dealing with this is to use a small pull down resistor, e.g., 500 ohms. In accordance with the modified embodiment a relatively small resistor R30, for example, a 2 watt resistor of 470 ohms, connects line W to AC ground. This will result in approximately twelve to fifteen milliamps which can still result in a wave form which has a hill in between consecutive highs when the thermostat line is closed. The addition of a 12 volt zener diode CR10 prevents turn on unless the voltage exceeds 12 volts so even if the electronic thermostat causes 20 milliamps there will only be seven or eight volts on the high side of the resistor R30 which will be insufficient to turn on diode CR10. Back to back zeners are not necessary since only the positive half of the wave form is considered as an input in the control of the present invention. This compatibility is achieved by modifying the FIG. 2 embodiment by a change in a resistor and the addition of a zener diode for the W and G signal lines. The two watt resistors can be accommodated conveniently by cutting a hole in the circuit board in alignment with each resistor to prevent overheating of the board. It is also preferable to add resistor R32 between


```

00053
00054
00055      * DEFINITIONS FOR PORTA
00056
00057 P 0000      0001      A PILOTFT EQU 1
00058 P 0000      0002      A MFGMODE EQU 2
00059 P 0000      0003      A MOOFTDLY EQU 3
00060
00061      * DEFINITIONS FOR OUTPUT BUFFER "OUTPUTS"
00062
00063 P 0000      0007      A LED EQU 7
00064
00065
00066
00030
00031
00032      *-----*
00033      *                      RAM STORAGE ORIGATION POINT
00034      *-----*
00035 A 00c0      ORG J1RAM      RAM LOCATIONS SCO - SFF
00036
00037      *-----*
00038      *                      RAM RESERVATION SECTION
00039      *-----*
00040
00041      INCLUDE D:\6805\PASH\2GF\INTERRNC.ASM INTERFACE RMB'S MODULE
00001      OPT NOL
00014      OPT L
00015
00016 A 00c0      01      A RTCLOCK RMB 1      1/4 DISTANCE OF 60 HZ WAVE
00017 A 00c1      01      A RTCNIBIT RMB 1      HIGH BITS TO THE TCR
00018 A 00c2      01      A LASTIN1 RMB 1      LAST INPUT READ IN
00019 A 00c3      01      A LASTIN2 RMB 1      LAST NONCONFORMING INPUT VALUE
00020 A 00c4      01      A NEWCNT RMB 1      LIMIT OF NON CONFORMING INPUTS
00021 A 00c5      01      A NEWSAME RMB 1      NUMBER OF CONSECUTIVE GOOD READS
00022 A 00c6      01      A NUMCHK RMB 1      NUMBER OF INPUT CYCLES TO COMPARE
00023 A 00c7      01      A INPUTS RMB 1      INPUTS TO PASS TO OTHER PROGRAMS
00024 A 00c8      01      A OUTPUTS RMB 1      OUTPUTS RECEIVED FROM APPLICATION
00025 A 00c9      01      A HZ60 RMB 1      60 HZ COUNTER
00026 A 00ca      01      A SEC60 RMB 1      1 SECOND SET BIT
00027 A 00cb      01      A PULSES RMB 1      PULSES LEFT TO BEFORE 1 SEC IS UP
00028 A 00cc      01      A CYCLEFT RMB 1      DEBOUNCED CYCLES LEFT BEFORE VALID
00029 A 00cd      0a      A RROMBYTE RMB 10      RAM IMAGE OF CRC CHECK
00030 A 00d7      02      A CRC RMB 2      CRC CHECK VALUE REGISTER
00031 A 00d9      01      A BITCNT RMB 1      BIT COUNTER REGISTER
00032 A 00da      01      A IRCNT RMB 1      NUMBER OF INTERRUPTS COUNTED WITHOUT MAIN
00033 A 00db      01      A TCSRMASK RMB 1      TCSR MASK REGISTER
00034 A 00dc      01      A NUMCHK2 RMB 1
00035 A 00dd      01      A NOISECNT RMB 1      NOISE INTERRUPT COUNTS
00042
00043      INCLUDE D:\6805\PASH\2GF\2GFRMBC.ASM 2GF RMB'S MODULE
00001      OPT NOL
00014      OPT L
00015
00016 A 00de      01      A FLAGREG1 RMB 1      INPUT FLAG REGISTERS
00017 A 00df      01      A FLAGREG2 RMB 1      OUTPUT FLAG REGISTERS
00018 A 00e0      01      A FLAGREG3 RMB 1      INDUCED DRAFT FLAG REG
00019 A 00e1      01      A MVOMREG RMB 1      MVOM REGISTER ADDRESS
00020 A 00e2      01      A GOFFREG RMB 1      GOFF REGISTER ADDRESS
00021 A 00e3      01      A IDOFFREG RMB 1      IND DFT REGISTER ADDRESS
00022 A 00e4      01      A MVOFFREG RMB 1      MVOFF REGISTER ADDRESS
00023 A 00e5      01      A TEST RMB 1      TEST CODE REGISTER
00024 A 00e6      01      A SWICTR RMB 1      SWI COUNTER REGISTER
00025 A 00e7      01      A O60CNTS RMB 1      MINUTE COUNTER
00026 A 00e8      01      A WDNCTR RMB 1      DLY ON DRAFT COUNTER
00027 A 00e9      01      A ST_TIMER RMB 1      PILOT DRAFT OPTION IDLE TIMER
00028 A 00ea      01      A ONTIMCTR RMB 1      PILOT DRAFT OPTION ON TIMER
00029 A 00eb      01      A GONCTR RMB 1      GONDLY COUNTER
00030 A 00ec      01      A HILOCNT1 RMB 1      TIME DELAY FOR AC DETERMINATION
00031 A 00ed      01      A HILOCNT2 RMB 1
00032 A 00ee      01      A MEMCHK RMB 1
00033 A 00ef      01      A INITEST RMB 1
00034
00044
00045      *-----*
00046      *                      CALCULATED CRC VALUE
00047      *-----*
00048
00049      INCLUDE D:\6805\PASH\2GF\CRCVALC.ASM CRC VALUE
00001      OPT NOL
00014      OPT L
00015
00016 A 0300      ORG S300

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00017 A 0300 0f46 A FDB S0F46 CRC VALUE
00050
00051
00052 *-----*
00053 * PROGRAM ORIGATION POINT (ROM) *
00054 *-----*
00055
00056 A 0302 ORG J1ROM ROM LOCATIONS S0300 - S06FF
00057
00058 *-----*
00059 * PROGRAM SECTION *
00060 *-----*
00061
00062 INCLUDE D:\6805\PASM\2GF\RAMCHKC.ASM RAM CHECK ROUTINE
00001 OPT NOL
00015 OPT L
00016
00017 *-----*
00018 * RAM VERIFICATION ROUTINE *
00019 *-----*
00020
00021 A 0302 9c RESETV RSP RESET STACK POINTER
00022 A 0303 5f CLRX
00023 A 0304 cf 07f0 A STX WDOG PET THE WATCH DOG
00024
00025 A 0307 a6 07 A LDA #7
00026 A 0309 b7 c6 A STA NUMCHK
00027 A 030b 3f ee A CLR MEMCHK
00028 A 030d ae ef A LDX #INITEST
00029 A 030f f6 RAM LDA ,X If the ram is scrambled, reinitilazite it,
00030 A 0310 bb ee A ADD MEMCHK
00031 A 0312 b7 ee A STA MEMCHK if not, then jump to calibration routine
00032 A 0314 5c INCX
00033 A 0315 3a c6 A DEC NUMCHK
00034 A 0317 27 02 031b BEQ CMPARE
00035 A 0319 20 f4 030f BRA RAM
00036
00037 A 031b b1 a6 A CMPARE CMP RAMTST
00038 A 031d 26 03 0322 BNE GO_ON
00039 A 031f cc 03ba A JMP INTEND
00040
00041 A 0322 a6 55 A GO_ON LDA #S55
00042 A 0324 ae c0 A RAMCHK4 LDX #J1RAM PUT RAM START ADDRESS IN INDEX
00043
00044 A 0326 f7 RAMCHK1 STA 0,X STORE ACCA IN RAM ADDRESS
00045 A 0327 f1 CMPA 0,X DOES THE RAM VALUE EQUATE TO THE
00046 A 0328 27 04 032e BEQ RAMCHK2 STORED VALUE?
00047 A 032a ae a0 A LDX #S40 LOAD FAILURE CODE
00048 A 032c 20 0b 0339 BRA RAMCHKEND END CHECK
00049
00050 A 032e 5c RAMCHK2 INCX
00051 A 032f 26 f5 0326 BNE RAMCHK1 IF INDEX DOES NOT TURN OVER TO S00
00052 * LOOP BACK TO RAMCHK1
00053
00054 A 0331 a1 aa A CMP #SAA IF ACCA IS =SAA, THEN THE ROUTINE
00055 A 0333 27 04 0339 BEQ RAMCHKEND IS COMPLETE!
00056
00057 A 0335 a6 aa A LDA #SAA CONTINUE THE TEST WITH SAA IN ALL RAM
00058 A 0337 20 eb 0324 BRA RAMCHK4 START OVER WITH NEW VALUE IN ACCA
00059
00060 A 0339 bf e5 A RAMCHKEND STX TEST
00063
00064 INCLUDE D:\6805\PASM\2GF\CRCHK.ASM CRC CHECK ROUTINE
00001 OPT NOL
00016 OPT L
00017
00018 * ROUTINE TO COPY ROM IMAGE INTO RAM
00019
00020 A 033b 5f CLRX
00021 A 033c d6 06d4 A NEXT LDA RROMIMAGE,X
00022 A 033f e7cd STA RROMBYTE,X
00023 A 0341 5c INCX
00024 A 0342 a3 0a A CMPX #10
00025 A 0344 23 f6 033c BLS NEXT
00026
00027 A 0346 3f d7 A GENCRC CLR CRC CRC=0
00028 A 0348 3f d8 A CLR CRC+1
00029 A 034a bd cd A GENCRC1 JSR RROMBYTE GET A BYTE OF ROM
00030 A 034c b8 d7 A EOR CRC CRC=CRC^(ROMBYTE<<8)
00031 A 034e b7 d7 A STA CRC
00032 A 0350 a6 08 A LDA #8 FOR(I=8,I=0,--I)
00033 A 0352 b7 d9 A STA BITCNT
00034 A 0354 5f CLRX PET THE WATCH DOG

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00035 A 0355 cf 07f0 A STX WDOG
00036
00037 A 0358 38 d8 A CRCCGEN2 LSL CRC-1 CRC=CRC<<1
00038 A 035a 39 d7 A ROL CRC
00039 A 035c 24 0c 036a BCC CRCCGEN3 WAS THE MS BIT OF OLD CRC=1?
00040 A 035e a6 21 A LDA #521 YES,CRC=CRC*51021
00041 A 0360 b8 d8 A EOR CRC+1
00042 A 0362 b7 d8 A STA CRC+1
00043 A 0364 a6 10 A LDA #510
00044 A 0366 b8 d7 A EOR CRC
00045 A 0368 b7 d7 A STA CRC
00046
00047 A 036a 3a d9 A CRCCGEN3 DEC BITCNT DONE FOR ALL 8 BITS OF NEW INPUT?
00048 A 036c 26 ea 0358 BNE CRCCGEN2 NO, CONTINUE
00049 A 036e b6 ce A LDA RROMBYTE+1 YES
00050 A 0370 a1 07 A CMA #507 HAVE WE GENED A CRC FOR ENTIRE ROM?
00051 A 0372 26 d6 034a BNE GENCRC1 NO, CONTINUE
00052
00053 A 0374 c6 0300 A LDA $300 LOAD 1ST BYTE OF CRC VALUE
00054 A 0377 b1 d7 A CMP CRC CMP TO CALCULATED CRC
00055 A 0379 26 07 0382 BNE CRCCGEN4 IF EQUAL CHECK SECOND BYTE
00056 A 037b c6 0301 A LDA $301 LOAD 2ND BYTE OF CRC VALUE
00057 A 037e b1 d8 A CMP CRC+1 CMP TO CALCULATED 2ND BYTE
00058 A 0380 27 06 0388 BEQ CRCCGEN5 IF EQUAL ROM GOOD
00059
00060 A 0382 a6 05 A CRCCGEN4 LDA #05 LOAD FAILURE CODE
00061 A 0384 bb e5 A ADD TEST ADD TO RAMTEST CODE
00062 A 0386 b7 e5 A STA TEST SAVE FINAL TEST CODE
00063
00064 CRCCGEN5
00065
00066 INCLUDE D:\6805\PM3M\2GF\INTERINC.ASM INTERFACE INITIALIZATION
00001 OPT MCL
00014 OPT L
00015
00016
00017 A 0388 3f c2 A CLR LASTIN1 USED IN INPUT MODULE
00018 A 038a 3f c3 A CLR LASTIN2
00019 AND APPLICATION MODULE
00020 A 038c 3f ca A CLR SEC60 USED IN INPUT MODULE FOR TIMING
00021 A 038e a6 3b A LDA #SIXTY
00022 A 0390 b7 e9 A STA WZ60 USED IN INPUT MODULE
00023 A 0392 b7 e7 A STA O60CMTS
00024 A 0394 3f cb A CLR PULSES USED IN INPUT MODULE
00025
00026 A 0396 3f c7 A CLR INPUTS CLEARS THE INPUTS MEMORY LOCATION
00027 A 0398 18 c7 A BSET 4,INPUTS SETS THE R/LIMIT INPUT ON
00028 A 039a 3f c8 A CLR OUTPUTS CLEARS THE OUTPUTS MEMORY LOCATION
00029 A 039c 3f e2 A CLR GOFFREG USED IN G/ECON ROUTINE
00030 A 039e 3f e3 A CLR IDOFFREG USED IN W.IMOFT ROUTINE
00031 A 03a0 3f e8 A CLR WOVCTR CLEAR THE DRAFT DELAY ON CTR
00032 A 03a2 3f e1 A CLR MVONREG USED IN MV ROUTINE
00033 A 03a4 3f e4 A CLR MVOFFREG USED IN MV ROUTINE
00034 A 03a6 3f de A CLR FLAGREG1 USED IN ALL ROUTINES
00035 A 03a8 3f df A CLR FLAGREG2 USED IN ALL ROUTINES
00036 A 03aa 3f e0 A CLR FLAGREG3 USED IN DRAFT ROUTINE
00037 A 03ac 3f e6 A CLR SWICTR CLEAR THE SWI COUNTER
00038 A 03ae 3f ea A CLR ONTIMCTR CLEAR PILOT DRAFT ON TIME CTR
00039 A 03b0 3f e9 A CLR ST_TIMER CLEAR PILOT DRAFT WAIT CTR
00040 A 03b2 3f eb A CLR GONCTR CLEAR G DELAY ON COUNTER
00041 A 03b4 3f 00 A CLR PORTA CLEAR PORTA PRIOR TO TURNING INTO OUTPUTS
00042
00043 A 03b6 5f CLRX
00044 A 03b7 cf 07f0 A STX WDOG
00045
00046 A 03ba a6 b3 A INITEND LDA #583
00047 A 03bc b7 db A STA TCSRMASK INITIALIZE TCSR MASK
00048 A 03be a6 13 A LDA #513
00049 A 03c0 b7 08 A STA TCSR INITIALIZE THE TCSR - TOFE DISABLED, RTIE
00050 ENABLED, AND RTI RATE 65.5ms
00051 A 03c2 3f 05 A CLR DDRB SET PORT B TO INPUTS
00052 A 03c4 a6 f0 A LDA #5FD
00053 A 03c6 b7 04 A STA DDRA SET PORT A TO PA0-3 INPUTS, PA4-7 OUTPUTS
00054 A 03c8 b6 c8 A LDA OUTPUTS
00055 A 03ca b7 00 A STA PORTA RESTORE OUTPUT DATA
00056
00057 A 03cc 3f c1 A CLR RTCHIBIT USED IN CALIBRATION MODULE
00058 A 03ce 3a e6 A DEC SWICTR DECREMENT SWI COUNTER TO START AT 5FF
00059
00060 INITIALIZE THE FAULT TOLERANCE REGS FOR INPUT ROUTINE
00061
00062 A 03d0 3f dd A CLR NOISECNT CLEAR NOISE COUNTER (COUNTS TO #20)
00063 A 03d2 3f da A CLR IRQCNT CLEAR THE INTERRUPT COUNTER
00064 A 03d4 a6 19 A LDA #FAULTS NUMBER OF NON-SAME READINGS PERMITTED

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00065 A 03d6 b7 c4 A STA NEWCNT WAITING FOR 55 OF THE IDENTICAL VALUE
00066 A 03d8 a6 08 A LDA #CONCNT NUMBER OF CONSECUTIVE SAME READINGS REQ'D
00067 A 03da b7 c5 A STA NEWSAME BEFORE STARTING A NEW INPUT VALUE
00068
00069 A 03dc a6 34 A LDA #52
00070 A 03de b7 dc A STA NUMCHK2
00071 A 03e0 b7 c6 A STA NUMCHK USED IN INPUT MODULE
00072 A 03e2 b7 cc A STA CYCLEFT USED IN INPUT MODULE
00073
00074 A 03e4 3f ec A CLR NILOCNT1
00075 A 03e6 3f ed A CLR NILOCNT2
00076
00077
00078 A 03e8 9c RSP RESET THE STACK POINTER
00067 MODULE
00068
00069 INCLUDE D:\6805\PASH\2GF\CALIB.C.ASM INTERFACE CALIBRATION
00001 OPT NOL
00016 OPT L
00017
00018 A 03e9 04 0045 0431 BRSET MFGMODE,PORTA,MFGTST IF RTI OCCURS THEN WE ARE MFG TEST
00019
00020 A 03ec 1d 08 A BCLR 6,TCSR CLEARS THE RTI FLAG
00021 A 03ee 2e fe 03ee CALIB BIL CALIB
00022 A 03f0 2f fe 03f0 TRANS BIH TRANS WAITS FOR A HIGH TO LOW TRANSITION
00023
00024 A 03f2 be 09 A LDX TCR LOAD & STORE REAL TIME CLOCK
00025 A 03f4 bf c0 A STX RTCLOCK THIS IS THE START TIME
00026 A 03f6 1f 08 A BCLR 7,TCSR MAKE SURE TOF BIT IS CLEARED
00027
00028 A 03f8 2f 09 0403 LOW BIH HIGH WAITS FOR A HIGH
00029 A 03fa 0f 08fb 03f8 BRCLR 7,TCSR,LOW WAIT FOR TOF TO GO HIGH
00030 A 03fd 1f 08 A BCLR 7,TCSR CLEARS THE TOF BIT AND THEN KEEPS TRACK
00031 A 03ff 3c c1 A INC RTCNIBIT OF THE HIGH BITS
00032 A 0401 20 f5 03f8 BRA LOW
00033
00034 A 0403 2e 09 040e HIGH BIL CALIBRATE WAITS FOR A LOW
00035 A 0405 0f 08fb 0403 BRCLR 7,TCSR,HIGH WAITS FOR TOF TO GO HIGH
00036 A 0408 1f 08 A BCLR 7,TCSR CLEARS THE TOF BIT AND THEN KEEPS TRACK
00037 A 040a 3c c1 A INC RTCNIBIT OF THE HIGH BITS
00038 A 040c 20 f5 0403 BRA HIGH
00039
00040 A 040e b6 09 A CALIBRATE LDA TCR LOADS FINISHED TIME LOWER BITS
00041
00042 A 0410 ae 06 A LDX #SIX 2*6 = 64 DIVIDE BY 64
00043 A 0412 34 c1 A AGAIN LSR RTCNIBIT MOVES NIBITS INTO LOW BITS
00044 A 0414 46 RORA WHILE DIVIDING
00045 A 0415 34 c0 A LSR RTCLOCK DIVIDES THE START TIME ALSO
00046 A 0417 5a DECC
00047 A 0418 26 f8 0412 BNE AGAIN
00048 A 041a b0 c0 A SUB RTCLOCK SUBTRACTS THE START TIME FROM THE FINISHED
00049 A 041c a1 10 A CMP RTCLOCK CLOCK VALUE LESS THAN MIN CLOCK ALLOWED
00050 A 041e 85 10 0430 BLO RTCLOCK IF YES, GO TO MWI
00051 A 0420 a1 90 A CMP RTCLOCK CLOCK VALUE GREATER THAN MAX CLOCK ALLOWED
00052 A 0422 32 0c 0430 BRI RTCLOCK IF YES, GO TO MWI
00053 A 0424 b7 c0 A STA RTCLOCK THIS IS 1/4 LENGTH OF 60K2, STORED 4 LATER
00054 A 0426 b7 cb A STA PULSES
00055 A 0428 2e fe 0428 HOLD1 BIL HOLD1 WAITS FOR BEGINNING OF NEXT WAVE BECAUSE
00056 A 042a 2f fe 042a HOLD2 BIH HOLD2 WHEN LEAVING AN INTERRUPT WILL OCCUR
00057 A 042c 0a CLI AS SO AS THE BIT IS CLEARED
00058 A 042d cc 04ab A JMP START
00059
00060 A 0430 83 BADCLOCK SWI
00061
00062
00063 * NOTE : INSTRUCTION SET TO FIND MIDPOINT SHOULD BE 64 INSTRUCTION *
00064 * CYCLES LONG INORDER TO FIND THE MIDPOINT. *
00065
00066
00067
00068 MODULE
00069
00070
00071
00072 INCLUDE D:\6805\PASH\2GF\2GFINTSTC.ASM 2GF BOARD TEST MONITOR
00001 OPT NOL
00021 OPT L
00022
00023 A 0431 a6 1e A MFGTST LDA #30 DETERMINE IF AC OR DC
00024 A 0433 b7 ed A STA NILOCNT2
00025 * LDA #3FF
00026 * STA NILOCNT1
00027
00028 A 0435 2f 45 047c MFGTST1 BIH ACTST
00029 A 0437 3a ec A DEC NILOCNT1
00030 A 0439 26 fa 0435 BNE MFGTST1
00031 A 043b 3a ed A DEC NILOCNT2

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00032 A 043d 26 f6 0435 BNE MFGTST1
00033
00034 A 043f 1d 08 A BCLR 6,TCSR CLEAR RTIF
00035 A 0441 10 00 A TSTYS BSET 0,PORTA TURN ON INDUCED DRAFT RELAY
00036 A 0443 0a 01fd 0443 GTST1 BRSET 5,PORTB,GTST1 WAIT FOR G=0
00037 CLRX
00038 STX MDOG PET THE WATCH DOG
00039 A 0446 3f c6 A CLR MUMCHK
00040 A 0448 3f 01 A CLR PORTB TURN ALL OFF BEFORE SETTING INS TO OUTS
00041 A 044a a6 1c A LDA #B1C SET UP R,V,MV AS OUTPUTS
00042 A 044c b7 05 A STA B0B8
00043 A 044e d6 06de A XFER LDA PWREV,X MOVE DATA INTO ACCUMULATOR USING X REGISTER
00044 AS INDEX TO TABLE OF DATA
00045 A 0451 ad 3c 048f BSR SERIAL SEND ACCUMULATOR TO TEST STATION
00046
00047 A 0453 5f CLRX
00048 A 0454 cf 07f0 A STX MDOG
00049
00050 A 0457 3c c6 A INC MUMCHK INCREMENT NUMBER OF BYTES TRANSFERRED
00051 A 0459 be c6 A LDX MUMCHK
00052 A 045b c3 06de A CPX PWREV COMPARE NUMBER OF BYTES XFER'D TO FIRST
00053 TABLE ENTRY (WHICH IS THE COUNT)
00054 A 045e 26 0a 044e BNE XFER ALL DONE; NO, CONTINUE XFER
00055 A 045f b6 c5 A LDA #B1C LOAD RESULTS OF SELF TEST INTO ACC
00056 A 0462 ad 2b 048f BSR SERIAL SEND ACC TO TEST STATION
00057 CLRX
00058 STX MDOG PET THE WATCH DOG
00059 A 0464 3f c6 A CLR MUMCHK
00060 A 0466 b6 c5 A LDA TEST RE-LOAD SELF TEST RESULTS FOR CHECK SUM
00061 A 0468 ab 06de A XFER PWREV,X AS INDEX FROM IN ACC; INCREMENT BY X
00062 A 046b 3c 06de A CPX PWREV COMPARE COUNT TO FIRST DATA ENTRY IN TABLE
00063 A 046e c3 06de A BNE CSUM ALL DONE; NO, CONTINUE TO ACCUMULATE
00064 A 046f 26 f7 0468 BSR SERIAL SEND ACC (CHECK SUM) TO TEST STATION
00065 A 0471 ad 1c 048f BSR SERIAL
00066
00067 A 0473 0a 01fd 0473 GTST2 BRSET 5,PORTB,GTST2 WAIT FOR G=0
00068 A 0476 3f 01 A CLR PORTB TURN ALL PORT B OUTS OFF
00069 A 0478 3f 05 A CLR B0B8 SET ALL PORTS TO INPUTS
00070 A 047a 3f 00 A CLR PORTA TURN INDUCED DRAFT OFF
00071 A 047c a6 01 A ACTST LDA #1 SET UP NEW TIME DELAYS
00072 A 047e b7 c6 A STA MUMCHK STORE NEW NUMBER OF INPUTS
00073 A 0480 b7 dc A STA MUMCHK2
00074 A 0482 b7 c9 A STA #Z60 STORE NEW CLOCK RATE
00075 A 0484 a6 b0 A LDA #S80
00076 CLRX
00077 STX MDOG PET THE WATCH DOG (X CLEARED ABOVE)
00078 A 0486 b7 db A STA TCSRMASK
00079 A 0488 1d 08 A BCLR 6,TCSR
00080 A 048a 3f cb A CLR PULSES
00081 A 048c cc 03ee A JMP CALIB RETURN TO NORMAL OPERATION WITH ALL
00082 TIMEOUTS DIVIDED BY 60
00083
00084
00085
00086
00087
00088
00089
00090
00091
00092
00093
00094
00095
00096
00097
00098
00099
00100

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*****
* THIS SUBROUTINE TRANSFERS DATA TO THE MFG TEST EQUIPMENT.
*
* 1) CONTENTS OF INDEX REGISTER MODIFIED
*
* 2) ACCUMULATOR CONTAINS THE BYTE TO BE TRANSFERED
*
* 3) BIT 4 OF PORT B IS THE MSB OF THE TWO BITS XFER'D
*
* 4) BIT 3 OF PORT B IS THE LSB OF THE TWO BITS XFER'D
*
* 5) BIT 5 OF PORT B = 0 INDICATES TEST STATION READY
* FOR MORE DATA
*
* 6) BIT 5 OF PORT B = 1 INDICATES THE TEST STATION HAS
* READ LAST DATA
*
* 7) BIT 2 OF PORT B IS SET WHEN NEW DATA IS AVAILABLE
* TO TEST STATION
*
* 8) BIT 2 OF PORT B IS CLEARED WHEN DATA IS BEING
* ALTERED
*****

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00101 A 048f ee 04 A SERIAL LDX #4 SET # OF 2 BIT XFERS
00102 A 0491 15 01 A BCLR 2,PORTB CLEAR BIT 2 OF PORTB: DATA CHANGING (MV)
00103 A 0493 0a 01fd 0493 GMAIT1 BRSET 5,PORTB,GMAIT1 WAIT FOR G=0
00104 A 0496 29 01 A BOLA CHECK FIRST BIT
00105 A 0497 24 02 049b BCC BIT1 FIRST BIT = 0
00106 A 0499 18 01 A BSET 4,PORTB NO, SET BIT 4 OF PORTB (R/LIMIT)
00107 A 049b 49 01 A BOLA CHECK SECOND BIT
00108 A 049c 24 02 04a0 BCC BIT2 SECOND BIT = 0
00109 A 049e 16 01 A BSET 3,PORTB NO, SET BIT 3 OF PORTB (V)
00110 A 04a0 14 01 A BIT2 BSET 2,PORTB SET BIT 2 OF PORTB : SIGNALS TEST STATION
00111 NEW DATA AVAILABLE
00112 A 04a2 0b 01fd 04a2 GMAIT2 BRCLR 5,PORTB,GMAIT2 WAIT FOR G=1
00113 A 04a5 3f 01 A CLR PORTB CLEAR PORT B OUTPUTS: DATA CHANGING
00114 A 04a7 5a DECC DECC DECREMENT NUMBER OF 2 BIT XFERS
00115 A 04a8 26 c9 0493 BNE GMAIT1 ALL 8 BITS XFER'D; NO, SEND MORE

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00116 A 04ea 81      RTS          ALL DONE: RETURN
00173
00174          INCLUDE D:\6805\PMASH\26F\26FRC.ASM 26F PROGRAM MODULE
00181          OPT  NOL
00184          OPT  L
00187
00188 A 04eb 1f  ca      A START.  BCLR 7,SEC60  CLEAR 60 HERTZ PRESENT FLAG
00189 A 04ed 1d  ca      A          BCLR 6,SEC60  CLEAR RT OPERATION FLAG
00190
00191 A 04ef 0f  cafd  04af STARTX BRCLR 7,SEC60,STARTX WAIT FOR 60 HERTZ PRESENT FLAG
00192 A 04ed 0d  cafa  04af BRCLR 6,SEC60,STARTX WAIT FOR RT OPERATION FLAG
00193
00194 A 04b5 5f          CLRX
00195 A 04b6 cf  07fd  A      STX  WDOG   RESET THE WATCH DOG TIMER
00196 A 04b9 bf  da      A      STX  IRQCNT CLEAR THE INTERRUPT COUNTER
00197
00198
00199          *****
00200          *  R/LIMIT ROUTINE  *
00201          *****
00202
00203 A 04bb 09  c706  04c4  BRCLR 4,INPUTS,R_OFF IS R ON?
00204 A 04ba 1e  de      A      BSET 7,FLAGREG1 IF ON, SET RFLAG=1
00205 A 04e8 1f  c8      A      BCLR 7,OUTPUTS TURN ON LED IF LIMIT IS CLOSED
00206 A 04c2 20  07      04cb  BRA  G_ECON
00207 A 04c4 1f  de      A R_OFF BCLR 7,FLAGREG1 IF OFF, SET RFLAG=0
00208 A 04c6 1e  c8      A      BSET 7,OUTPUTS TURN ON LED IF LIMIT IS OPEN
00209 A 04c8 cd  064b  A      JSR  CLRDRFT
00210
00211
00212
00213          *****
00214          *  G/ECON ROUTINE  *
00215          *****
00216
00217 A 04cb 0b  c716  04e4  G_ECON BRCLR 5,INPUTS,R_OFF IS G_ECON ON?
00218 A 04ca 0a  e008  04d9  BRSET MONFLAG,FLAGREG3,#DLYON
00219 A 04d1 1a  e0      A      BRSET MONFLAG,FLAGREG3
00220 A 04d5 a6  04      A      LDA  #DLY
00221 A 04d5 b7  ab      A      STA  MONCTR
00222 A 04d7 20  20      04f9  BRA  W_INDOFT
00223
00224
00225 A 04d9 0c  de1d  04f9  #DLYON BRSET #FLAG1,FLAGREG1,W_INDOFT DELAY ON ROUTINE
00226 A 04dc 3d  -db      A      IST  #DLY
00227 A 04de 26  79      04f9  BNE  W_INDOFT
00228 A 04d0 1c  de      A      BRSET #FLAG1,FLAGREG1
00229 A 04e2 20  15      04f9  BRA  W_INDOFT
00230
00231
00232 A 04e4 0b  e00a  04f1  G_OFF BRCLR MONFLAG,FLAGREG3,G_CTR IF #FLAG1=0 GO CHECK COUNTER
00233 A 04e7 14  de      A      BRSET #FLAG1,FLAGREG1 SET #FLAG2=1
00234 A 04e9 1b  e0      A      BCLR #FLAG1,FLAGREG3 SET #MONFLAG=0
00235 A 04eb a6  3c      A      LDA  #DLY
00236 A 04ed b7  e2      A      STA  MONCTR LOAD G_OFF COUNTER
00237 A 04ef 20  08      04f9  BRA  W_INDOFT
00238
00239
00240 A 04f1 3d  e2      A G_CTR TST  MONCTR TEST COUNTER FOR ZERO COUNT
00241 A 04f3 26  04      04f9  BNE  W_INDOFT IF NOT ZERO, BRANCH TO NEXT ROUTINE
00242 A 04f5 1b  de      A      BCLR 5,FLAGREG1 SET #FLAG2=0
00243 A 04f7 1d  de      A      BCLR #FLAG1,FLAGREG1
00244
00245          *****
00246          *  W_INDOFT ROUTINE  *
00247          *****
00248
00249 A 04f9 07  c71b  0517  W_INDOFT BRCLR 3,INPUTS,W_OFF IS W_INDOFT ON?
00250
00251 A 04fc 00  e008  0507          BRSET MONFLAG,FLAGREG3,W_DLYON HAS THE W FLAG ALREADY BEEN SET?
00252
00253 A 04ff 10  e0      A      BSET MONFLAG,FLAGREG3 SET FLAG FOR W ON STATE
00254 A 0501 a6  04      A      LDA  #IDLYON INITIALIZE DELAY ON TIMER
00255 A 0503 b7  e8      A      STA  MONCTR
00256 A 0505 20  33      053a  BRA  W_END
00257
00258
00259 A 0507 02  e058  0562  W_DLYON BRSET WOFFLAG1,FLAGREG3,WV BRANCH TO END IF DELAY ON IS COMPLETE
00260 A 050a 3d  e8      A      TST  MONCTR HAS THE DELAYON COUNTER TIMED OUT?
00261 A 050c 26  2c      053a  BNE  W_END
00262
00263
00264 A 050e 12  e0      A      BSET WOFFLAG1,FLAGREG3
00265
00266
00267 A 0510 cd  064b  A      JSR  CLRDRFT
00268 A 0513 3f  e9      A      CLR  ST_TIMER
00269 A 0515 20  23      053a  BRA  W_END
00270
00271
00272

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00096 A 0517 01 e013 052d W_OFF BRCLR WOFFLAG,FLAGREG3,W_DLYOFF IF FLAG IS NOT SET GO TO DLYOFF
00097 A 051a 03 e00a 0527 BRCLR WOFFLAG1,FLAGREG3,SWORT_W
00098
00099 A 051d e6 1c A LDA #DLYOFF INITIATE ID DELAY OFF TIMER
00100 A 051f b7 e3 A STA IDOFFREG
00101 A 0521 14 e0 A BSET WOFFLAG2,FLAGREG3 SET STATE FLAG FOR W OFF AND
00102 A 0523 11 e0 A BCLR WOFFLAG,FLAGREG3 DLEAY TIME OFF
00103 A 0525 20 13 053a BRA W_END
00104
00105 A 0527 3f e8 A SWORT_W CLR WOFFCTR CLEAR DELAY ON COUNTER
00106 A 0529 11 e0 A BCLR WOFFLAG,FLAGREG3 CLEAR THE W ON FLAG
00107 A 052b 20 0d 053a BRA W_END
00108
00109 A 052d 06 0002 0532 W_DLYOFF BRSET WOFFDLY,PORTA,CTR_OFF IS THE DELAY OFF BYPASSED?
00110 A 0530 3f e3 A CLR IDOFFREG RESET THE DELAY OFF COUNTER
00111
00112 A 0532 3d e3 A CTR_OFF TST IDOFFREG IS THE DELAY OFF COUNTER=0?
00113 A 0534 26 04 053a BNE W_END
00114
00115 A 0536 13 e0 A BCLR WOFFLAG1,FLAGREG3
00116 A 0538 15 e0 A BCLR WOFFLAG2,FLAGREG3
00117
00118
00119 * TINED PILOT DRAFT OPTION ROUTINE *
00120
00121
00122
00123 A 053a 02 0025 0562 W_END BRSET PILOTDF,PORTA,MV IS THE OPTION TAB REMOVED??
00124 A 053d 02 e022 0562 BRSET WOFFLAG1,FLAGREG3,MV BYPASS ROUTINE IF DRAFT IS
00125 * ALREADY ON
00126
00127 A 0540 06 e008 054b BRSET STRTIMER,FLAGREG3,WAIT_ON HAS THE WAIT PERIOD STARTED?
00128
00129 A 0543 a6 3c A LDA #WAITIME INITIALIZE THE WAIT PERIOD TIMER
00130 A 0545 b7 e9 A STA ST_TIMER AND SET THE MODE FLAG
00131 A 0547 16 e0 A BSET STRTIMER,FLAGREG3
00132 A 0549 20 17 0562 BRA MV
00133
00134 A 054b 3d e9 A WAIT_ON TST ST_TIMER TIME UP YET??
00135 A 054d 26 13 0562 BNE MV
00136
00137 A 054f 08 e008 055a BRSET ONFLAG,FLAGREG3,ITS_ON HAS THE DRAFT ON MODE STARTED?
00138
00139 A 0552 18 e0 A BSET ONFLAG,FLAGREG3 INITIATE DRAFT ON MODE
00140 A 0554 a6 78 A LDA #ONTIME
00141 A 0556 b7 ea A STA ONTIMCTR
00142 A 0558 20 08 0562 BRA MV
00143
00144 A 055a 3d ea A ITS_ON TST ONTIMCTR
00145 A 055c 26 04 0562 BNE MV
00146
00147 A 055e 19 e0 A BCLR ONFLAG,FLAGREG3
00148 A 0560 17 e0 A BCLR STRTIMER,FLAGREG3
00149
00150
00151 * MV ROUTINE *
00152
00153
00154 A 0562 05 c719 057e MV BRCLR 2,INPUTS,MV_OFF IF MV=0,BRANCH TO MV_OFF
00155
00156 A 0565 cd 064b A JSR CLMDRAFT
00157
00158 A 0568 00 de08 0573 BRSET 0,FLAGREG1,MVDLYON IF MVOFFLAG=1 BRANCH TO MVDLYON
00159 A 056b 10 de A BSET 0,FLAGREG1 SET MVOFFLAG=1
00160 A 056d a6 1e A LDA #MVDLY
00161 A 056f b7 e1 A STA MVDLYREG INITIATE MVDLY TIMER
00162 A 0571 20 20 0593 BRA OUTPUT
00163
00164 A 0573 04 de1d 0593 MVDLYON BRSET 2,FLAGREG1,OUTPUT IF MVOFFLAG1=1 BRANCH TO OUTPUT
00165 A 0576 3d e1 A TST MVDLYREG MVDLYCTR=0?
00166 A 0578 26 19 0593 BNE OUTPUT MVDLYCTR NOT =0,THEN BRANCH TO OUTPUT
00167 A 057a 14 de A BSET 2,FLAGREG1 SET MVOFFLAG1=1
00168 A 057c 20 15 0593 BRA OUTPUT
00169
00170 A 057e 01 de0a 058b MV_OFF BRCLR 0,FLAGREG1,MVDLYOFF IF MVOFFLAG=0,BRANCH TO MVDLYOFF
00171 A 0581 12 de A BSET 1,FLAGREG1 SET MVOFFLAG2=1
00172 A 0583 11 de A BCLR 0,FLAGREG1 SET MVDLY=0
00173 A 0585 a6 b4 A LDA #MVDLYOFF
00174 A 0587 b7 e4 A STA MVDLYOFFREG INITIATE MVDLYOFF COUNTER
00175 A 0589 20 08 0593 BRA OUTPUT

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00176
00177 A 058b 3d e4 A MVOLYOFF TST MVOFFREG IF MVOFFDLY COUNTER NOT = 0
00178 A 058d 26 04 0593 BNE OUTPUT BRANCH TO OUTBUF
00179 A 058f 13 de A BCLR 1,FLAGREG1 MVOFFFLAG2=0
00180 A 0591 15 de A BCLR 2,FLAGREG1 MVOFFFLAG1=0
00181
00182 *****
00183 * OUTPUT FLAG ROUTINE
00184 *****
00185
00186 A 0593 b6 de A OUTPUT LDA FLAGREG1
00187 A 0595 a4 60 A AND %COOLMASK
00188 A 0597 27 06 059f BEQ CLOFFLAG IF GFLAG1=0 AND GFLAG2=0
00189 * THEN BRANCH TO CLOFFLAG
00190 A 0599 14 df A BSET 2,FLAGREG2 NT_CLFLAG=1, COOL FAN ON
00191 A 059b 17 df A BCLR 3,FLAGREG2 CL_NTFLAG=0, HEAT FAN OFF
00192 A 059d 20 14 05b3 BRA OUTBUF
00193
00194 A 059f 15 df A CLOFFLAG BCLR 2,FLAGREG2 NT_CLFLAG=0, COOL FAN OFF
00195
00196 A 05a1 b6 de A LDA FLAGREG1
00197 A 05a3 a4 87 A AND %HEATMASK
00198
00199 A 05a5 a1 81 A CMP %HEAT1 IF FLAGREG1=100X X001
00200 A 05a7 27 08 05b1 BEQ NTOFFLAG THEN TURN HEAT OFF
00201
00202 A 05a9 a1 80 A CMP %HEAT2 IF FLAGREG1=100X X000
00203 A 05ab 27 04 05b1 BEQ NTOFFLAG THEN TURN HEAT OFF
00204
00205 A 05ad 16 df A BSET 3,FLAGREG2 CL_NTFLAG=1, HEAT FAN ON
00206 A 05af 20 02 05b3 BRA OUTBUF TURN HEAT ON
00207
00208 A 05b1 17 df A NTOFFLAG BCLR 3,FLAGREG2 CL_NTFLAG=0, HEAT FAN OFF
00209
00210 *****
00211 * OUTPUT BUFFER ROUTINE
00212 *****
00213 *
00214 * THIS ROUTINE ONLY RUNS ONCE EVERY SECOND
00215 * IT IS BASED ON THE ONE SECOND CLOCK BIT THAT IS TOGGLED
00216 * IN THE "1" RST ROUTINE
00217 *
00218
00219 A 05b3 01 ca7e 0634 OUTBUF BRCLR 0,SEC60,IND_DFT IF SECOND FLAG IS NOT SET
00220 * BRANCH TO END OF TIMER ROUTINE
00221 A 05b6 11 ca A BCLR 0,SEC60 CLEAR SECONDS FLAG
00222
00223 A 05b8 05 df0f 05ca BRCLR 2,FLAGREG2,HEAT IF NT_CLFLAG=0, BRANCH TO HEAT
00224 A 05bb 01 df06 05c4 BRCLR 0,FLAGREG2,HEATOFF IF TIMEOUT1=0, BRANCH TO HEATOFF
00225
00226 A 05be 1c c8 A BSET 6,OUTPUTS *** TURN COOL FAN ON ****
00227
00228 A 05c0 13 df A BCLR 1,FLAGREG2 TIMEOUT2=0
00229 A 05c2 20 24 05e8 BRA TIMERS
00230
00231 A 05c4 19 c8 A HEATOFF BCLR 4,OUTPUTS *** TURN HEAT FAN OFF ***
00232
00233 A 05c6 10 df A BSET 0,FLAGREG2 TIMEOUT1=1
00234 A 05c8 20 1e 05e8 BRA TIMERS
00235
00236 A 05ca 07 df0f 05dc HEAT BRCLR 3,FLAGREG2,ALLOFF IF CL_NTFLAG=0, BRANCH TO ALLOFF
00237 A 05cd 03 df06 05d6 BRCLR 1,FLAGREG2,COOLOFF IF TIMEOUT2=0, BRANCH TO COOLOFF
00238
00239
00240 A 05d0 18 c8 A BSET 4,OUTPUTS *** TURN HEAT FAN OFF ***
00241
00242 A 05d2 11 df A BCLR 0,FLAGREG2 TIMEOUT1=0
00243 A 05d4 20 12 05e8 BRA TIMERS
00244
00245 A 05d6 1d c8 A COOLOFF BCLR 6,OUTPUTS *** TURN COOL FAN OFF ***
00246
00247 A 05d8 12 df A BSET 1,FLAGREG2 TIMEOUT2=1
00248 A 05da 20 0c 05e8 BRA TIMERS
00249
00250 A 05dc 19 c8 A ALLOFF BCLR 4,OUTPUTS *** TURN OFF HEAT FAN ***
00251 A 05de 1d c8 A BCLR 6,OUTPUTS *** TURN OFF COOL FAN ***
00252
00253 A 05e0 3d e6 A TST SWICTR TEST THE SWI COUNTER FOR ZERO
00254 A 05e2 26 04 05e8 BNE TIMERS IF NOT ZERO, BRANCH TO TIMERS
00255 A 05e4 0e c801 05e8 BRSET 5,OUTPUTS,TIMERS IF IND_DFT IS ON, BRANCH TO TIMERS
00256 A 05e7 83 * SWI IF ALL FANS ARE OFF, AND THE SWICTR
00257 * EQUALS ZERO, THEN RESET/CALIBRATE
00258

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00259
00260
00261
00262
*****
*   TIMERS           ROUTINE
*****
00263 A 05e8 01 de0c 05f7 TIMERS BRCLR WOFFFLAG,FLAGREG1,G_DLYON
00264 A 05eb 00 e009 05f7 BRSET WOFFFLAG,FLAGREG3,G_DLYON
00265 A 05ee 0e c804 05f5 BRSET 5,OUTPUTS,LEDOFF
00266 A 05f1 1e c8 A BRSET LED,OUTPUTS
00267 A 05f3 20 02 05f7 BRA G_DLYON
00268
00269 A 05f5 1f c8 A LEDOFF BCLR LED,OUTPUTS
00270
00271
00272 A 05f7 0b e005 05ff G_DLYON BRCLR WOFFFLAG,FLAGREG3,G_DLYOFF
00273 A 05fa 0c de02 05ff BRSET GFLAG1,FLAGREG1,G_DLYOFF
00274 A 05fd 3a eb A DEC GONCTR
00275
00276 A 05ff 0b de02 0604 G_DLYOFF BRCLR 5,FLAGREG1,ID_DLY DEC G DELAY REG IF GFLAG2=1
00277 A 0002 3a e2 A DEC GOFFREG
00278
00279 A 0004 01 e005 060c ID_DLY BRCLR WOFFFLAG,FLAGREG3,WOODYOFF HAS THE W FLAG BEEN SET?
00280 A 0607 02 e002 060c BRSET WOFFLAG1,FLAGREG3,WOODYOFF IS THE DRAFT FAN ON FLAG SET?
00281
00282 A 060a 3a e8 A DEC WONCTR
00283
00284 A 060c 05 e002 0611 WOOLYOFF BRCLR WOFFLAG2,FLAGREG3,PILOT_DLY
00285 A 060f 3a e3 A DEC IDOFFREG
00286
00287 A 0611 07 e011 0625 PILOT_DLY BRCLR STRTIMER,FLAGREG3,MV_DLYON IS THE SYSTEM IN WAIT MODE?
00288 A 0614 08 e00c 0623 BRSET ONFLAG,FLAGREG3,PILOT_ON IS THE DRAFT ON CYCLE ACTIVE?
00289
00290 A 0617 3a e7 A DEC 060CNTS
00291 A 0619 26 0a 0625 BNE MV_DLYON
00292
00293 A 061b 3a e9 A DEC ST_TIMER DECREMENT DRAFT OFF TIMER ONCE A MINUTE
00294 A 061d a6 3c A LDA #60
00295 A 061f b7 e7 A STA 060CNTS
00296 A 0621 20 02 0625 BRA MV_DLYON
00297
00298 A 0623 3a ea A PILOT_ON DEC ONTIMCTR
00299
00300 A 0625 01 de05 062d MV_DLYON BRCLR 0,FLAGREG1,MV_DLYOFF
00301 A 0628 04 de02 062d BRSET 2,FLAGREG1,MV_DLYOFF
00302 A 062b 3a e1 A DEC MVOFFREG DEC MVOFFDLY IF MVOFFLAG=1 AND
00303 MVOFFFLAG=0
00304
00305 A 062d 03 de02 0632 MV_DLYOFF BRCLR 1,FLAGREG1,SWINT
00306 A 0630 3a e4 A DEC MVOFFREG DEC MVOFFDLY IF MVOFFLAG2=1
00307
00308 A 0632 3a e6 A SWINT DEC SWICTR DEC THE SWI COUNTER EVERY SECOND
00309
00310
00311
*****
*   INDUCED-DRAFT-TIME-OFF-Routine
*****
00312
00313
00314
00315 A 0634 b6 de A IND_DFT LDA FLAGREG1
00316 A 0636 a4 81 A AND #10000000000000000000 FLAGREG1 %1000 0001
00317 A 0638 a1 80 A CMP #10000000000000000000 FLAGREG1 %1000 0000
00318 A 063a 26 06 0642 BNE ID_ON IF YES, TURN OFF ID FAN
00319
00320 A 063c b6 e0 A LDA FLAGREG3 BNE FLAGREG3 3B001 0010
00321 A 063e a4 12 A AND #10000000000000000000 FLAGREG3
00322 A 0640 27 04 0646 BEQ ID_OFF
00323
00324
00325 A 0642 1a c8 A ID_ON BSET 5,OUTPUTS *** IF NO, TURN ID FAN ON ***
00326
00327 A 0644 20 02 0648 BRA ID_END
00328
00329 A 0646 1b c8 A ID_OFF BCLR 5,OUTPUTS *** TURN ID FAN OFF ***
00330
00331 A 0648 cc 04ab A ID_END JMP START
00332
*****
*   SUBROUTINE TO CLEAR DRAFT WAIT TIME
*****
00333
00334
00335
00336
00337
00338
00339 A 064b 17 e0 A CLRDRFT BCLR STRTIMER,FLAGREG3
00340 A 064d 19 e0 A BCLR ONFLAG,FLAGREG3
00341 A 064f 3f ea A CLR ONTIMCTR
00342 A 0651 3f e9 A ST_TIMER

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00343 A 0653 e6 3c A LDA #60
00344 A 0655 b7 e7 A STA 060CNTS
00345 A 0657 81 A RTS
00346
00347
00075
00076 INCLUDE D:\6805\PMASH\2GF\INPUTC.ASM INTERFACE INPUT MODULE
00001 OPT NOL
00015 OPT L
00016
00017 A 0658 1e ca A IROV BSET 7,SEC60 SET 60 HERTZ PRESENT FLAG
00018
00019 A 065a b6 da A LDA IROVNT THIS LIMITS THE NUMBER OF INTERRUPTS THAT
00020 A 065c 4c da A INCA CAN BE COUNTED WITHOUT THE CONTROL PROGRAM
00021 A 065d a1 14 A CMP #20 BEING EXECUTED
00022 A 065f 24 67 06c8 BNS RET
00023
00024 A 0661 b7 da A STA IROVNT
00025 A 0663 b6 c0 A LDA RTCLKVAL LOAD THE RTCLKVAL VALUE
00026
00027 A 0665 ae 09 A LOOP1 LDX #9 2 CYC-DELAY
00028 A 0667 9d 09 A BOP 2 CYC-DELAY
00029 A 0668 5a 09 A LOOP BECX 3 CYC-DELAY
00030 A 0669 26 fd 0668 BNE LOOP 3 CYC-DELAY
00031 A 066b 4a fd 0668 BECA 3 CYC-DELAY
00032 A 066c 26 f7 0665 BNE LOOP1 3 CYC-DELAY: ONE COMPLETE LOOP=64 CYC
00033
00034
00035 A 066e b6 01 A LDA PORTB WE ARE NOW AT MID POINT READ INPUTS
00036
00037
00038 A 0670 02 010d 0680 BRSET 1,PORTB,FAULT IF C INPUT IS HIGH THEN INPUT MUST BE OUT
00039 OF SYNCH, GO TO FAULT COUNT
00040
00041 A 0673 05 0016 068c BRCLR 2,PORTA,NORMOP CONTINUE WITH NORMAL OPERATION IF MFG TEST
00042 INPUT REMAINS LOW
00043
00044
00045 A 0676 b7 c7 A STA INPUTS IN ACCEL. TEST MODE, ALWAYS UPDATE INPUTS
00046
00047 A 0678 a6 13 A LDA #19 SWI generated if out of synch one time
00048 A 067a b7 dd A STA NOISECNT
00049
00050 A 067c 1c ca A BSET 6,SEC60
00051 A 067e 20 46 06c6 BRA FAST
00052
00053
00054 A 0680 b6 dd A FAULT LDA NOISECNT ALLOW 20 NOISE INTERRUPTS BEFORE RESETTING
00055 A 0682 4c dd A INCA DO NOT CHANGE INPUT COUNTERS
00056 A 0683 a1 14 A CMP #20
00057 A 0685 24 04 068b BNS STRTOVR IF NOISECNT=20 GO TO SWI
00058 A 0687 b7 dd A STA NOISECNT
00059 A 0689 20 3d 06c8 BRA RET
00060
00061 A 068b 83 STRTOVR SWI
00062
00063
00064 A 068c b1 c2 A NORMOP CMP LASTIN1 CHECK IF THEY ARE THE SAME AS LAST LOAD
00065 A 068e 26 08 0698 BNE NEWIN1 IF YES, HAS THERE BEEN 60 READS
00066
00067 A 0690 3a cc A DEC CYCLEFT CHECKS FOR 60 INPUTS CONSECUTIVELY
00068 A 0692 26 28 06bc BNE SECONDS IF 60 READS HAVEN'T OCCURED GO UPDATE CLOCK
00069
00070 A 0694 b7 c7 A STA INPUTS IF 60 READS HAVE OCCURED UPDATE INPUTS MEM.
00071 A 0696 20 18 06b0 BRA RESET1
00072
00073 A 0698 3a c4 A NEWIN1 DEC NEWCNT
00074 A 069a 27 14 06b0 BEQ RESET1
00075
00076 A 069c b1 c3 A CMP LASTIN2 START OVER LOOKING FOR 60 READS CONSEC.
00077 A 069e 26 0c 06ac BNE NEWIN2
00078
00079 A 06a0 3a c5 A DEC NEWAME
00080 A 06a2 26 18 06bc BNE SECONDS
00081
00082 A 06a4 b7 c2 A STA LASTIN1
00083 A 06a6 b6 dc A LDA NEWCNT
00084 A 06a8 b7 cc A STA CYCLEFT
00085 A 06aa 20 08 06b4 BRA RESET2
00086
00087 A 06ac b7 c3 A NEWIN2 STA LASTIN2
00088 A 06ae 20 08 06b8 BRA LOWNAME
00089

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00090 A 06b0 b6 c6 A RESET1 LDA #NUNCK NUNCK+1 NUMBER OF CONSECUTIVE READS DESIRED
00091 A 06b2 b7 cc A STA CYCLEFT NUMBER OF READ LEFT BEFORE CONSIDERED O.K.
00092
00093 A 06b4 a6 19 A RESET2 LDA #FAULTS REINITIALIZE ALL CNTS
00094 A 06b6 b7 c4 A STA #CNTCNT
00095 A 06b8 a6 08 A LDW#SAME LDA #DCONCNT INITIALIZE THE # OF READS REQ'D TO UPDATE
00096 " " " " LAST INPUT REG.
00097 A 06ba b7 c5 A STA #NEWNAME
00098
00099 A 06bc 3c cb A SECONDS INC PULSES #Z60 KEEPS TRACK OF 1 SECOND TIME
00100 A 06be b6 c9 A LDA #Z60 60 CYCLES IS 1 SECOND
00101 A 06c0 b1 cb A CMP PULSES HAS 1 SECOND ELAPSED
00102 A 06c2 26 04 06c8 BNE RET IF NOT EQUAL THEN GET OUT OF ROUTINE
00103
00104 A 06c4 3f cb A CLR PULSES
00105 A 06c6 10 ca A FAST BSET 0,SEC60 IF EQUAL THEN SET BIT TO SHOW ONE SEC.
00106
00107 A 06c8 80 RET RTI
00077
00078 INCLUDE D:\6805\PASH\2GF\OUTPUT.ASM INTERFACE OUTPUT MODULE
00001 OPT NOL
00015 OPT L
00016
00017 A 06c9 b6 c8 A TIMERV LDA OUTPUTS LOAD THE OUTPUTS TO SET
00018 A 06cb b7 00 A STA PORTA
00019 A 06cd a6 13 A LDA #B13 TCSRMASK LOAD THE TCSR
00020 " AND TCSR RESET RTIF
00021 A 06cf b7 08 A STA TCSR
00022 A 06d1 1c ca A BSET 6,SEC60 SET REAL TIME CLOCK OPERATING PROPERLY
00023 A 06d3 80 RTI RETURN FROM THE INTERRUPT
00079
00080 INCLUDE D:\6805\PASH\2GF\RRORBYTE.ASM CRC ROM IMAGE
00001 OPT NOL
00014 OPT L
00016
*****
* RRORBYTE SUBROUTINE *
*****
* ROM IMAGE OF RAM ROUTINE
*****
00021 A 06d4 c6 0302 A RRIMAGE LDA #302
00022 A 06d7 3c cf A INC RRORBYTE+2
00023 A 06d9 26 02 06dd BNE RRIMAGE1
00024 A 06db 3c ce A INC RRORBYTE+1
00025 A 06dd 81 RRIMAGE1 RTS
00001
00002 INCLUDE D:\6805\PASH\2GF\ZGFPHCPD.ASM ZGF PART NUMBER AND
00001 OPT NOL
00014 OPT L
00015
00016 A 06de 07 A PHREV FCB #07 NUMBER OF DIGITS IN PH AND REV
00017 A 06df 35 A FCC 5,39270 PART NUMBER
00018 A 06e4 41 A FCC 1,A REVISION LEVEL
00019
00020 A 06e5 40 A FCC 6,8TEXAS COPYRIGHT NOTICE
00021 A 06eb 20 A FCC 12, INSTRUMENTS " "
00022 A 06f7 30 A FCC 8,09-19-91 COPYRIGHT DATE
00023 " COPYRIGHT MODULE
00024
00025 A 06ff 01 A DCB #ROMEND-?+1,383 FILL REMAINING ROM
00026 " LOCATIONS WITH SWI's
00027
*****
* PART NUMBER, COPYRIGHT, MOR (OPTIONAL), AND VECTORS SETUP SECTION *
*****
00089
00090
00091
00092 * INCLUDE D:\6805\PASH\2GF\J2MOR.ASM
00093
00094 A 07f8 ORG J1VCTRS
00095
00096 INCLUDE D:\6805\PASH\2GF\J1VCTRS.ASM J1 TIMER, IRQ, SWI, AND
00001 OPT NOL
00014 OPT L
00015
00016 A 07f8 06c9 A FDB TIMERV TIMER VECTOR
00017 A 07fa 0658 A FDB IREQV INTERRUPT REQUEST VECTOR
00018 A 07fc 0302 A FDB RESETV SOFTWARE INTERRUPT VECTOR
00019 A 07fe 0302 A FDB RESETV RESET INTERRUPT VECTOR
00097 "
00098 RESET VECTORS MODULE
00099
END

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STRTIMER	EGU	A 0005	3:45	127	131	148	287	339														
STRTOVR		A 000b	19:61	57																		
ST_TIMER		A 0009	5:27	39	92	130	134	293	342													
SWICTR		A 0006	5:24	37	58	253	308															
SWINT		A 0032	17:308	305																		
TCR	EGU	A 0009	2:24	24	40																	
TCR	EGU	A 0008	2:22	49	20	26	29	30	35	36	34	79	21									
TCRPMASK		A 000b	4:33	47	78																	
TEST		A 00e5	5:23	60	61	62	55	60														
TIMERS		A 05a8	14:263	229	234	243	248	254	255													
TIMERV		A 06c9	20:17	16																		
TRANS		A 03f0	9:22	22																		
TSTYES		A 0441	10:35																			
WDLTOFF		A 040c	17:284	279	280																	
WAITIME	EGU	A 003c	3:21	129																		
WAIT_ON		A 054b	14:134	127																		
WDOG	EGU	A 07f0	2:25	23	35	44	48	25														
WDFLAG1	EGU	A 0001	3:43	85	89	97	115	124	280													
WDFLAG2	EGU	A 0002	3:44	101	116	284																
WDMCTR		A 00a8	5:26	31	82	86	105	282														
WDMFLAG	EGU	A 0000	3:42	78	80	96	102	106	264	279												
W_DLYOFF		A 052d	13:109	96																		
W_DLYON		A 0507	13:85	78																		
W_END		A 053a	13:123	83	87	93	103	167	113													
W_FINDOFT		A 06f9	13:76	52	54	56	58	65	68													
W_OFF		A 0517	13:96	76																		
XFER		A 044e	10:43	54																		

We claim:

1. Apparatus for controlling the energization of a main blower fan motor and an induced draft fan motor based on low voltage AC input signals comprising transformer means for providing a selected low voltage AC power supply from a line voltage AC power source having a selected frequency, means for providing a 5 volt DC power supply.

microprocessor means having input ports including an interrupt IRQ port and output ports and having a real time clock, the microprocessor means powered by the 5 volt DC power supply, low voltage input signal lines connected to the input ports and adapted to provide the low voltage AC input signals to the input ports,

relays having contacts relatively movable into and out of engagement with one another in response to selected low voltage AC input signals to the input ports of the microprocessor means, the contacts adapted to energize high power lines coupled to the main blower fan motor and the induced draft fan motor,

the low voltage AC power supply of the transformer means having an AC voltage common connected to the IRQ port, means to detect the falling edge of the AC voltage common wave at the IRQ port and, after a delay of a quarter of an AC wave length, to read the signals at the input ports,

and, in response to the signals at the input ports, means to energize the relay contacts from an output signal at the microprocessor means based on the real time clock so that the output signal is asynchronous relative to the AC power line frequency.

2. Apparatus according to claim 1 in which the low voltage AC input signals are 24 volt signals and are each coupled to the input ports of the microprocessor means through a current limiting resistor and selected low voltage AC input signals are connected to the AC voltage common through a pull down resistor.

3. Apparatus according to claim 2 in which the current limiting resistor is 100K ohms.

4. Apparatus according to claim 2 in which the output signal include a high speed signal on a high speed signal line and a low speed signal on a low speed signal

25 line for the main blower fan motor and an induced draft fan signal on an induced draft fan signal line.

5. Apparatus according to claim 4 further including a zener diode serially connected to the input ports to prevent conduction of current to the input ports below a selected level.

6. Apparatus according to claim 2 further including relay driver means interconnected between the output ports and the relays.

7. Apparatus according to claim 2 in which one of the low voltage AC input signals is for a main valve input, the main valve input being connected to the AC power source through a pull up resistor.

8. Apparatus according to claim 1 including means to periodically calibrate the reading of the input ports to assure that the reading is synchronous with the AC power source.

9. Apparatus according to claim 1 in which the low voltage AC input signals are read at the peak of the AC input signal.

10. Apparatus according to claim 9 in which the input ports are read a selected number of times before the microprocessor means generates an output.

11. Apparatus according to claim 1 in which selected time delays determined by the real time clock are provided in the microprocessor means before an output is generated to energize a selected relay.

12. Apparatus according to claim 1 in which the main blower fan motor has a cool speed winding and a heat speed winding and separate relays for energizing each speed winding, the heat speed winding having a selected time delay on and a selected time delay off.

13. Apparatus according to claim 12 in which the cool speed winding is energized instantly upon generating a low voltage AC input signal and has a selected time delay off.

14. Apparatus according to claim 13 in which a low voltage AC input signal for the cool speed winding overrides a low voltage AC input signal for the heat speed winding.

15. Apparatus according to claim 13 in which the induced draft fan motor has a selected time delay off.

16. The method of controlling a system having a main blower fan motor with heat and cool speed windings

and an induced draft fan motor responsive to input signals from a thermostat calling respectively for energization of the heat and cool speed windings and energization of the induced draft fan motor, the system having a microprocessor means for receiving the input signals and for generating output signals, the microprocessor means having an IRQ interrupt port and a real time clock, the system having transformer means for transforming line AC voltage to 24 volt AC power for the input signals including a transformer common, rectified 24 VAC power to energize relays and 5 volt DC power to power the microprocessor means, and respective separate relays for energizing the heat and cool speed windings and the induced draft fan motor in response to the output signals from the microprocessor means, the method comprising the steps of:

- coupling the transformer common to the IRQ interrupt port,
- executing a sub-routine on each falling edge of an AC voltage common wave on the transformer common,
- the sub-routine comprising the step of waiting one quarter of a wave of the AC voltage common wave and then reading the input signals to the microprocessor means so that the input signals are read at the peak of the AC wave of the input signals synchronously with the AC voltage,
- generating an output signal by the microprocessor means in response to respective input signals and the read time clock to coupled the 24 volt DC power to a selected relay asynchronously to the line AC voltage.

17. The method of controlling a system according to claim 16 including the step of calibrating the reading of input signals each time the system is energized by finding an edge of the AC voltage common wave form, counting the real time clock cycles in one complete AC line cycle and deriving one quarter of a wave time period.

18. The method of controlling a system according to claim 17 in which the step of calibrating is performed on a periodic basis every few seconds.

19. The method of controlling a system according to claim 16 including the step of calibrating the reading of input signals on a periodic basis every few seconds that

the system is energized by finding an edge of the AC voltage common wave form, counting the real time clock cycles in one complete AC line cycle and deriving one quarter of a wave time period.

20. Apparatus for controlling the energization of a load based on low voltage AC input signals comprising transformer means for providing a selected low voltage AC power supply from a line voltage AC power source having a selected frequency, means for providing a 5 volt DC power supply.

microprocessor means having input ports including an interrupt IRQ port and output ports and having a real time clock, the microprocessor means powered by the 5 volt DC power supply, low voltage input signal lines connected to the input ports and adapted to provide the low voltage AC input signals to the input ports,

relay means having contacts relatively movable into and out of engagement with one another in response to selected low voltage AC input signals to the input ports of the microprocessor means, the contacts adapted to energize high power lines coupled to the load,

the low voltage AC power supply of the transformer means having an AC voltage common connected to the IRQ port, means to detect the falling edge of the AC voltage common wave at the IRQ port and, after a delay of a quarter of an AC wave length, to read the signals at the input ports,

the low voltage AC input signals being coupled to the input ports of the microprocessor means through current limiting resistors and selected input signals being connected to the AC voltage common through a pull down resistor, and, based on the input signals at the input ports, means to energize the relay contacts from an output signal of the microprocessor means.

21. Apparatus according to claim 20 in which the low voltage AC input signals are 24 volt signals and the current limiting resistor is 100K ohms.

22. Apparatus according to claim 20 in which one of the input signals is for a main valve input, the main valve input being connected to the AC power supply through pull up resistor.

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