Application Report
SLAA423–December 2009

XOSC8 Guidance

MSP430

ABSTRACT

MSP430 erratum XOSC8 places an extra consideration upon the crystal oscillator design beyond that found in the crystal oscillator design guide, *MSP430 32-kHz Crystal Oscillators* (SLAA322). Specifically, the erratum requires that the crystal oscillator circuit provides a minimum level of impedance to force the MSP430 oscillator circuit to work harder. This can be done with increased load capacitance, increased ESR, or by placing a resistor from the crystal input to ground.

Each of these workarounds has potential side effects that impact the crystal-oscillator circuit. A positive side effect is increased noise immunity. The negative side effects include increased power consumption and a decrease in the safety factor. With the decrease in safety factor, the maintenance of an acceptable safety factor becomes more challenging.

Due to the numerous factors that influence the crystal-oscillator circuit it is not possible to recommend a solution that works in all situations. This application report discusses the different components of the crystal oscillator circuit that can be used to mitigate XOSC8, as well as workarounds and the implications of each. The workarounds include choosing a larger ESR crystal and using a shunt resistance on the oscillator input.

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1 Introduction

The LFXT1 OSC circuit regulates the amount of energy supplied to the crystal-oscillator circuit. The intent of this regulation is to provide the smallest amount of energy to the circuit that still maintains oscillation. The benefits are to provide larger amounts of energy at start-up to improve reliability and reduce the amount of energy to maintain the oscillation during operation.

The energy associated with the oscillator circuit is directly related to the energy provided to the comparator, which converts the analog oscillation into the digital clock LFXT1. When the energy supplied to the oscillator is decreased, the energy is also decreased to the comparator. If the decrease is large enough, then the comparator does not recognize a valid analog input. The crystal-oscillator circuit is still functional, but the coupling between the analog circuit and the digital clock (LFXT1) is broken. This can be typically seen as a failure to meet the 30% duty cycle data sheet specification for ACLK or the stopping of ACLK. This bug is referred to as XOSC8:

XOSC8	LFXT1 Module
Function	ACLK failure when crystal ESR is below 40 kΩ
Description	When ACLK is sourced by a low-frequency crystal with an ESR below 40 kΩ, the duty cycle of ACLK may fall below the specification; the OFIFG may become set or, in some instances, ACLK may stop completely.
Workaround	Use a crystal with an ESR greater than 40 kΩ.

The performance of the comparator is affected by the temperature, V_{CC}, and the energy required for oscillation. The amount on energy required for oscillation is impacted by the board layout, the crystal ESR, and the load capacitance seen by the oscillator. As a reference point, the discussion in this document is based upon a board layout that is in accordance with *MSP430 32-kHz Crystal Oscillators* (SLAA322). With the board layout being 'held constant', the other parameters are varied to show the impact of each. The worst corner case is low temperature, high V_{CC}, low ESR, and low load capacitance. ESR and load capacitance are the most easily controlled by the designer and are the basis for the workarounds provided in this application report

2 Contribution of ESR, Load Capacitance, V_{CC}, and Temperature

V_{CC} and temperature are more related to the occurrence of XOSC8 while the ESR and load capacitance impact both the occurrence of XOSC8 and the oscillation allowance of the crystal-oscillator circuit.

2.1 Crystal ESR

In the 2xx and 4xx family of devices that exhibit XOSC8, the increase in crystal ESR causes an increase in oscillator output in an attempt to maintain the same level of oscillation allowance (robustness). This provides the flexibility to choose higher ESR crystals without significantly impacting operation. While unintentional, this is extremely important in addressing XOSC8, where a higher ESR crystal is recommended.

Table 1 shows the parameters of several crystals tested. Testing with test crystal 1a at -40°C resulted in failures for all combinations of V_{CC} and load settings. The failure rate was approximately 1%.

Table 1. Crystal Parameters for Test Crystals

Test Crystal	f_s (Hz)	F_L(nom) (Hz)	R_M (Ω)	L_M (H)	C_M (fF)	C_0 (pF)	C_L(nom) (pF)
1a	32762.83	32768.000	16331.20	7506.01	3.14	2.05	7.92
1b	32762.972	32768.000	13907.60	8985.880	2.626	2.004	6.552
2	32763.917	32768.000	41128.600	9626.190	2.451	1.689	8.147

When the same units are tested with test crystal 2, there were no failures for the 10-pF and 12.5-pF load cases. This confirms the higher resistance crystal (R_M > 40 kΩ) requirement found in the XOSC8 erratum, but also indicates the importance of using the correct or greater load capacitance.

2.1.1 ESR and Start-Up Reliability

The crystal ESR is directly related to the oscillator allowance and safety factor. Both the oscillator allowance and safety factor are figures of merit used to establish a level of reliability of the crystal-oscillator start-up. Typically, choosing a low-ESR crystal is done to improve the start-up time and reliability. Conversely, choosing a high-ESR crystal or adding a series resistance within the circuit increases the start-up time and decreases reliability.

The MSP430 data sheet provides the typical values of oscillator allowance for the LFXT1 module shown in Table 2:

Table 2. Oscillator Allowance

PARAMETER		TEST CONDITIONS	TYP	UNIT
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 6 pF	500	kΩ
		XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 12 pF	200	

Using equation (5) from *MSP430 32-kHz Crystal Oscillators* (SLAA322), the change in safety factor by increasing the ESR by 15 to 20 kΩ still results in a safe qualification (see Table 3).

Table 3. Change in Safety Factor (SF)

Safety Factor (SF) = OA/ESR		
SF Original	200 kΩ / 25 kΩ	8
SF New	200 kΩ / 45 kΩ	4.4

2.1.2 ESR Specification

Most crystal data sheets specify a typical and maximum ESR value for the crystal. For those vendors that do not provide a typical value, a good rule of thumb is 15 kΩ below the maximum. For example, if the vendor specifies a 50-kΩ maximum, the typical ESR is probably on the order of 35 kΩ, while a 60-kΩ maximum ESR crystal is typically on the order of 45 kΩ and above the erratum requirement.

Taking the 50-kΩ (maximum) ESR crystal in the pervious example and adding 10 to 15 kΩ of series resistance does not address the XOSC8 erratum. ESR is a function of the mechanical losses due to vibration (R_M), parasitic capacitance of the package (C_0), and the required load capacitance (C_L) (see equation 1 in *MSP430 32-kHz Crystal Oscillators* (SLAA322)). In some cases, applying as much as 90 kΩ or greater series resistance was required to prevent the XOSC8 failure with a 14-kΩ ESR crystal (crystal 1b) instead of simply adding 26 kΩ to reach the 40-kΩ requirement. The impact of adding such a large series resistance is a decreased safety factor as well as an increased start-up time.

2.2 Load Capacitance

A larger load capacitance value significantly reduces the probability of a failure even if the ESR condition is not met and V_{CC} and temperature are at the worst case conditions. The failure rate for test crystal 3a, at -40°C, with 0-pF, 6-pF, and 10-pF loads was 17%, 15%, and 2% respectively. Once the load capacitance was increased to 12.5 pF, the failure rate became 0%. Similarly, the failure rate was 0% when crystal 3b was tested with a 10-pF load (see Table 4).

Table 4. Crystal Parameters for Crystal 3a, 3b

Test Crystal	f_s (Hz)	F_L(nom) (Hz)	R_M (Ω)	L_M (H)	C_M (fF)	C_0 (pF)	C_L(nom) (pF)
3a Citizen	32761.488	32768.000	26753.600	8506.470	2.774	1.416	5.563
3b (Microcrystal)	32765.367	32768.000	34247.900	10816.200	2.181	1.061	12.511

Increasing the load capacitance beyond the recommended loading of the crystal results in a frequency error. This is further described in *MSP430 LFXT1 Oscillator Accuracy* (SLAA225). Also see the crystal manufacturer's data sheet.

It is highly recommended to use at least the minimum load capacitance for the crystal. The load capacitance settings used in this testing are the internal load settings of the MSP430. External capacitance can be used to achieve the same loading. Using too small or no load capacitance is not recommended. Using both internal and external load capacitors is also not recommended.

2.3 Temperature and V_{CC}

Failures with low ESR crystals were not completely eliminated by increasing temperature and decreasing V_{CC}. Therefore, bounding V_{CC} and temperature is not considered an effective workaround and is not recommended.

3 Using a Shunt Resistor From XIN to GND

An alternative to increasing the ESR or load capacitance to increase the power output of the oscillator is to apply a shunt resistance between the oscillator input pin (XIN) and ground (AV_{SS}). Retesting crystal 1a (ESR = 14 kΩ) with a load capacitance of 6 pF, the failure rate was improved to 0% with the addition of a 750-kΩ shunt resistor. The addition of the shunt resistance had very little impact and the safety factor was still 'very safe' (greater than 5).

Generally, the impedance of the shunt resistance should increase with the ESR of the crystal until the crystal exceeds 40 kΩ, at which point the shunt resistance should be removed (infinite impedance).

4 Failsafe Mechanisms

4.1 2xx Family

The OFIFG fault flag can be used to detect an LFXT1 fault caused by XOSC8. In the event of an LFXT1 oscillator failure the MSP430 can be switched to the VLO to maintain (a slower) operation. Software handling can also be put in place to transfer operation back to the LFXT1 once the fault is cleared.

4.2 4xx Family

The 4xx family does not provide another low-frequency source for ACLK, such as the VLO in the 2xx family. The ACLK can be monitored in software with the use of a timer resource to verify either the frequency or the duty cycle. In either case, this information can be used to 'decouple' the DCO from ACLK by turning off the FLL within the FLL+ module. The software can continue to monitor the ACLK and turn the FLL back on once the ACLK returns to regular operation.

5 Summary

The occurrence of XOSC8 can be controlled with V_{CC}, temperature, load capacitance, ESR, and impedance. However, only ESR and impedance adjustments provide solutions over the entire V_{CC} and temperature range. It is recommended to use the highest amount of load capacitance possible, regardless of the workaround chosen. Using too little or no load capacitance is not recommended. The first workaround is the workaround found in the XOSC8 erratum: Use a crystal with an ESR greater than 40 kΩ. The second workaround is to use a shunt or load resistor from XIN to ground (AV_{SS}).

The workarounds and discussions within this application report are based upon good design practices for low-frequency crystal oscillator circuits found in *MSP430 32-kHz Crystal Oscillators* (SLAA322). While disregarding good practices can actually mitigate the occurrence of XOSC8 (forcing the oscillator to work harder), doing so makes the impedance and capacitance values discussed in this report inapplicable.

6 References

1. *MSP430 32-kHz Crystal Oscillators* (SLAA322)

2. *MSP430 LFXT1 Oscillator Accuracy* (SLAA225)

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