

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Application of Jed Margolin

Serial No.: 11/130,939

Examiner: Phung M. Chung

Filed: 05/17/2005

Art Unit: 2117

For: MEMORY WITH INTEGRATED PROGRAMMABLE CONTROLLER

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENTS AND RESPONSE

Dear Sir:

In the Office Action mailed December 28, 2007, Claims 1-3, 5-6, 8, and 10-11 were allowed and Claims 14-16 were rejected. Please enter the following amendments and consider the following remarks.

Amendments to the claims begin on page 2 of this response. Remarks begin on page 7 of this response.

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Claim Amendments

Please cancel claims 14-16 without prejudice.

Claim 1. (previously presented) A single chip memory comprising:

- (a) a memory array;
- (b) a processor;
- (c) a processor RAM memory;
- (d) a multiplexor;

whereas:

- (a) said processor is connected to said processor RAM memory and said multiplexor;
- (b) said memory array is also connected to said multiplexor;
- (c) said memory array is a read/write memory;

whereby:

- (a) said multiplexor controls and arbitrates access between said memory array, said processor, said processor RAM memory, and a user's system;
- (b) said user's system uses said multiplexor to store a program into said processor RAM memory;
- (c) said processor uses said program in said processor RAM memory to test said memory array; and

whereas said program is an algorithmic test program.

Claim 2. (previously presented) The single chip memory of claim 1 further comprising a non-volatile memory connected to said processor, said processor RAM memory, and said multiplexor.

Claim 3. (previously presented) The single chip memory of claim 1 further comprising a programmable clock connected to said processor.

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2 Claim 4. (canceled)

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4 Claim 5. (previously presented) The single chip memory of claim 1 whereby said program is
5 also used by said processor to perform one or more functions selected from a group comprising
6 data pattern matching, moving data, graphics primitives, data encryption, and data decryption.

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8 Claim 6. (previously presented) A single chip memory comprising:

9 (a) a memory array;

10 (b) a processor;

11 (c) a processor RAM memory;

12 (d) a multiplexor;

13 (e) a non-volatile memory;

14

15 whereas:

16 (a) said processor is connected to said processor RAM memory, said multiplexor, and said
17 non-volatile memory;

18 (b) said memory array is also connected to said multiplexor;

19 (c) said memory array is a read/write memory;

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21 whereby:

22 (a) said multiplexor controls and arbitrates access between said memory array, said
23 processor, said processor RAM memory, said non-volatile memory, and a user's system;

24 (b) said user's system uses said multiplexor to store a program into said processor RAM
25 memory;

26 (c) said processor uses said program in said processor RAM memory to test said memory
27 array;

28 (d) said processor uses said non-volatile memory to store the results of said program in said
29 processor RAM memory used to test said memory array; and

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31 whereas said program is an algorithmic test program.

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2 Claim 7. (canceled)

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4 Claim 8. (previously presented) The single chip memory of claim 6 further comprising a
5 programmable clock connected to said processor.

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7 Claim 9. (canceled)

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9 Claim 10. (previously presented) The single chip memory of claim 6 whereby said program is
10 also used by said processor to perform one or more functions selected from a group comprising
11 data pattern matching, moving data, graphics primitives, data encryption, and data decryption.

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2 Claim 11. (previously presented) A single chip memory comprising:

- 3 (a) a memory array;
- 4 (b) a processor;
- 5 (c) a processor RAM memory;
- 6 (d) a multiplexor;
- 7 (e) a non-volatile memory;
- 8 (f) a programmable clock;

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10 whereas:

- 11 (a) said processor is connected to said processor RAM memory, said multiplexor, and said
- 12 non-volatile memory;
- 13 (b) said memory array is also connected to said multiplexor;
- 14 (c) said memory array is a read/write memory;
- 15 (d) said programmable clock is connected to said processor;

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17 whereby:

- 18 (a) said multiplexor controls and arbitrates access between said memory array, said
- 19 processor, said processor RAM memory, said non-volatile memory, and a user's system;
- 20 (b) said user's system uses said multiplexor to store a program into said processor RAM
- 21 memory;
- 22 (c) said processor uses said program in said processor RAM memory to test said memory
- 23 array;
- 24 (d) said processor uses said non-volatile memory to store the results of said program in said
- 25 processor RAM memory used to test said memory array; and

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27 whereas said program is an algorithmic test program.

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29 Claim12. (canceled)

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31 Claim13. (canceled)

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2 Claim 14. (canceled)

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4 Claim 15. (canceled)

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6 Claim 16. (canceled)

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REMARKS

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In the Office Action mailed December 28, 2007, Claims 1-3, 5-6, 8, and 10-11 were allowed and Claims 14-16 were rejected.

Applicant has canceled Claims 14-16 and therefore submits that the application as amended is in condition for allowance.

Respectfully submitted,

/Jed Margolin/ Date: January 24, 2008

Jed Margolin

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