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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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11/130,939                      05/17/2005                      Jed Margolin                      4359

23497                      7590                      06/25/2007  
JED MARGOLIN  
1981 EMPIRE ROAD  
RENO, NV 89521-7430

EXAMINER

CHUNG, PHUNG M

ART UNIT                      PAPER NUMBER

2117

MAIL DATE                      DELIVERY MODE

06/25/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Office Action Summary**

Application No.

11/130,939

Applicant(s)

MARGOLIN, JED

Examiner

Phung My Chung

Art Unit

2117

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1)  Responsive to communication(s) filed on \_\_\_\_\_.
- 2a)  This action is **FINAL**.
- 2b)  This action is non-final.
- 3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4)  Claim(s) 1-16 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5)  Claim(s) \_\_\_\_\_ is/are allowed.
- 6)  Claim(s) 1-16 is/are rejected.
- 7)  Claim(s) \_\_\_\_\_ is/are objected to.
- 8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9)  The specification is objected to by the Examiner.
- 10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All   b)  Some \*   c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1)  Notice of References Cited (PTO-892)
- 2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3)  Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 5/17/05
- 4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5)  Notice of Informal Patent Application
- 6)  Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC § 112***

1. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1, 6 and 11, lines 2-4, "a) a memory array;

b) a processor; and

c) a processor RAM memory" the interconnection and/or interrelation between these elements are unknown and what are they for?. Appropriate correction is required.

As per claims 2-5, 7-10, 12-13, these claims are also rejected because they dependent upon the rejected base claim.

As per claim 14, lines 2-4, "a) providing a memory array;

b) providing a processor; and

c) providing a processor RAM memory" the interrelation between these steps are unknown and what they are for? Appropriate correction is required.

As per claims 15-16, these claims are also rejected because they dependent upon the rejected base claim.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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3. Claims 1-2, 6-7, 11-12 and 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Shelton et al (6,035,380).

As per claim 1, Shelton et al disclose a single chip integrated circuit, comprising:

a memory array (102);

(b) a processor (701);

(c) a processor RAM memory (705);

(d) a multiplexor (1202);

whereas said multiplexor controls and arbitrates access between said memory array, said processor, said processor RAM memory, and a user's system. (See Figs. 11 and 12, col. 11, lines 22-45 and col. 12, lines 10-65).

As per claim 2, Shelton et al further comprising a non-volatile memory (704).

As per claims 6, 11 and 14, these claims are rejected under similar rationale as set forth in claim 1.

As per claims 7, 12 and 15, these claims are rejected under similar rationale as set forth in claim 2.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3, 8, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shelton et al (6,035,380) in view of Fulks et al (4,194,113).

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As per claim 3, the teaching of Shelton et al have been discussed above. Shelton et al further disclose a clock circuit (Fig. 14). They do not disclose that the clock circuit is a programmable clock. However, Fulks et al disclose a programmable clock (153). (See Fig. 5, col. 14, lines 53-68). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the programmable clock as taught by Fulks et al into the clock circuit of Shelton et al so that it can produce a high speed programmable clock signals utilized to control the operation of a high speed processor (HSP). (See col. 14, lines 53-68).

As per claims 8, 13 and 16, these claims are rejected under similar rationale as set forth in claim 3.

6. Claims 4-5, and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shelton et al (6,035,380) and further in view of Jarboe, Jr. et al (7,155,637).

As per claims 4-5, the teaching of Shelton et al have been discussed above. They do not disclose that a program is used by the processor to test the memory array. However, Jarboe, Jr. et al disclose that the program is used by the processor to test the memory array (col. 5, lines 53-63). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the program that is used by the processor to test the memory array as taught by Jarboe, Jr. et al into the invention of Shelton et al so that test program can be used to test memory array to detect errors and the test program can be stored in the processor RAM memory for later used.

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As per claims 9-10, these claims are rejected under similar rationale as set forth in claims 4-5.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Phung My Chung  
Primary Patent Examiner  
Art Unit 2117