

### OVERVIEW

The PLL0305A is a PLL synthesizer LSI fabricated using NPC's original molybdenum-gate CMOS technology. The input frequency divider ratio can be set by externally inputting serial data. The reference frequency divider ratio can be selected from 8 choices stored in the built-in ROM.

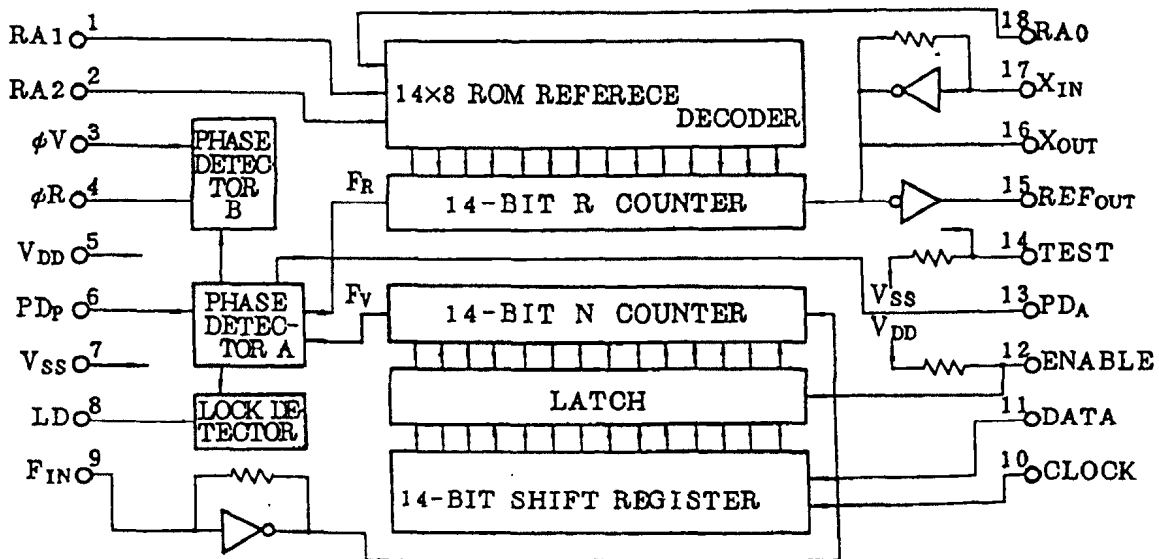
### FEATURES

- 30 MHz (5 V,  $F_{IN}$ )
- 15 MHz (5 V,  $X_{IN}$ )
- Reference frequency divider ratios  
16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- Input frequency divider ratios  
5 to 16383
- Lock detector pin
- Can be used with active or passive filters

### APPLICATIONS

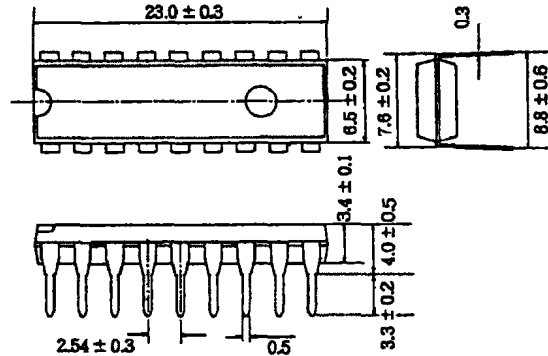
- Scanning receivers
- Amateur radios
- Radios
- Other

### BLOCK DIAGRAM



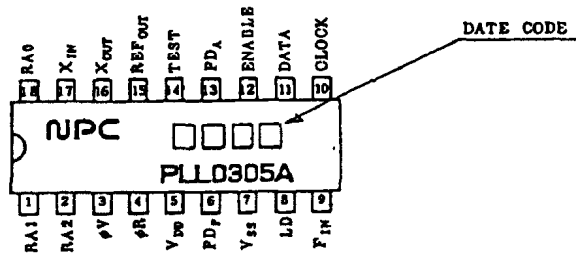
### PACKAGE DIMENSIONS

Unit: mm

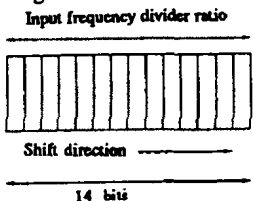


### PINOUT

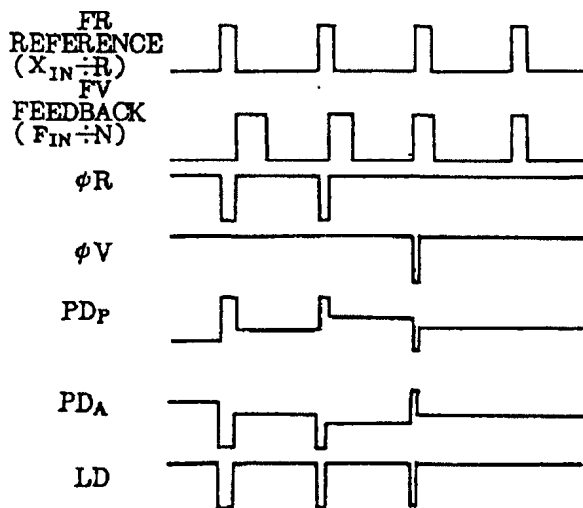
TOP VIEW



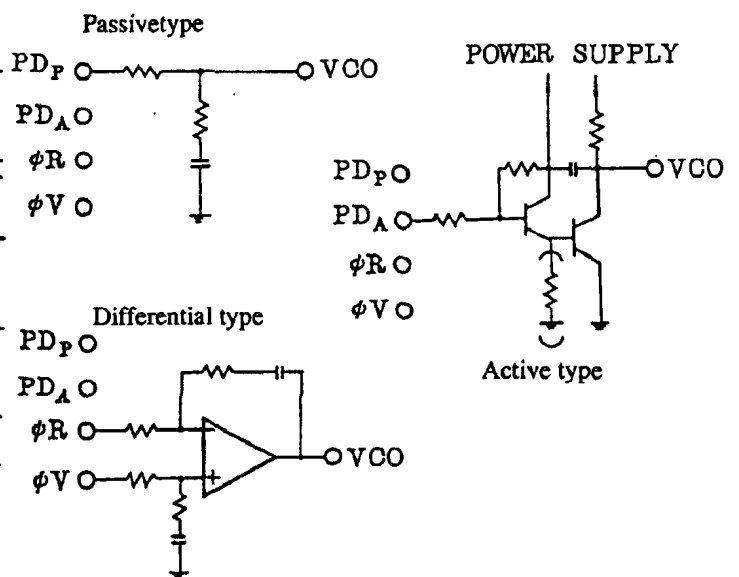
■ PIN DESCRIPTION

NAME (No.)	DESCRIPTION	NAME (No.)	DESCRIPTION																																				
RA0 (18) RA1 (1) RA2 (2)	Input pins used to select the reference frequency divider ratio from the table. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>RA2</th> <th>RA1</th> <th>RA0</th> <th>Divider ratio</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>16</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>512</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1024</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>2048</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>3668</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>4096</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>6144</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>8192</td></tr> </tbody> </table>	RA2	RA1	RA0	Divider ratio	0	0	0	16	0	0	1	512	0	1	0	1024	0	1	1	2048	1	0	0	3668	1	0	1	4096	1	1	0	6144	1	1	1	8192	CLOCK (10) DATA (11)	Shift register data and clock input. Data shifts by 1 bit when CLOCK changes from "L" to "H". The shift register configuration is shown below. Make the input data format coincide with the shift register configuration. 
RA2	RA1	RA0	Divider ratio																																				
0	0	0	16																																				
0	0	1	512																																				
0	1	0	1024																																				
0	1	1	2048																																				
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1	0	1	4096																																				
1	1	0	6144																																				
1	1	1	8192																																				
øV (3) øR (4) PD <sub>P</sub> (6) PD <sub>A</sub> (6) PD <sub>Δ</sub> (13)	Outputs for a lowpass filter. PDP and PDA are single-ended, tristate outputs. Connect the filter in use to the corresponding output pin. PD <sub>P</sub> .... passive filter PD <sub>A</sub> .... active filter øV, øR .... differential filter	ENABLE (12)  TEST (14)	Latch write signal. When "H", writing is enabled. Internal pull-up resistor.  Test pin. Should be left open during normal operation. Internal pull-down resistor.																																				
V <sub>DD</sub> (5)	Power supply 4.5 to 5.5 V	REF <sub>OUT</sub> (15)	Buffered reference oscillator (X <sub>IN</sub> , X <sub>OUT</sub> ) output. Recommend to connect a load to this pin for stable oscillation.																																				
V <sub>SS</sub> (7)	Ground	X <sub>OUT</sub> (16) X <sub>IN</sub> (17)	Pin for a quartz crystal oscillator. Internal feedback resistor is provided for AC coupling. Input an external clock to the X <sub>IN</sub> pin via a capacitor.																																				
LD (8)	Unlock detection. When unlocked, it is "L." When locked, it is "H."																																						
FIN (9)	Input frequency divider (N COUNTER) input. Internal feedback resistor for AC coupling.																																						

■ PHASE DETECTOR TIMING CHART



■ LOWPASS FILTER



■ ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply voltage	V <sub>DD-VSS</sub>	-0.3 to +7.0	V
Input voltage	V <sub>IN</sub>	V <sub>SS</sub> -3.0 to V <sub>DD</sub> +0.3	V
Operating temperature	T <sub>OPR</sub>	-30 to +80	°C
Storage temperature	T <sub>STG</sub>	-40 to +125	°C
Soldering temperature	T <sub>SLD</sub>	260±5	°C
Soldering time	t <sub>SLD</sub>	10	Sec

Setup time, hold time

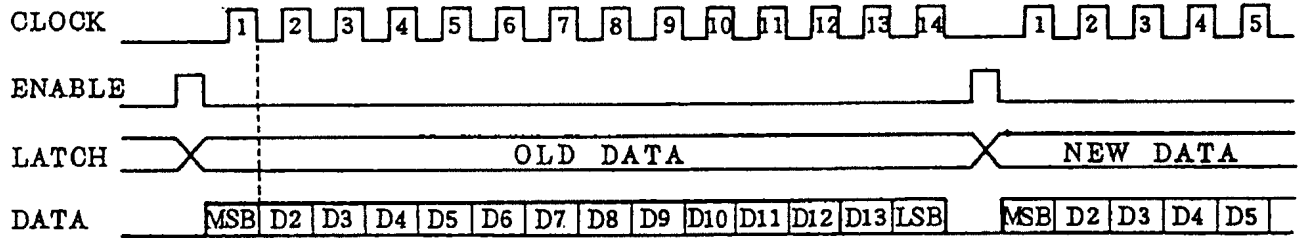
■ ELECTRICAL CHARACTERISTICS

V<sub>SS</sub> = 0V, V<sub>DD</sub> = 4.5 to 5.5V, T<sub>a</sub> = -30 to +80 °C

ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT	REMARKS
			MIN	TYP	MAX		
Supply voltage	V <sub>DD</sub>		4.5		5.5	V	
Current consumption	I <sub>DD</sub>	F <sub>IN</sub> =sine wave 30MHz 500mV <sub>p-p</sub> X <sub>IN</sub> =sine wave 15MHz 1V <sub>p-p</sub>		4.0	8.0	mA	* Output pin open
Maximum operating frequency 1	F <sub>MAX1</sub>	F <sub>IN</sub> =sine wave 500mV <sub>p-p</sub>	30	50		MHz	F <sub>IN</sub>
Maximum operating frequency 2	F <sub>MAX2</sub>	X <sub>IN</sub> =sine wave 1V <sub>p-p</sub>	15	50		MHz	X <sub>IN</sub>
Input voltage	V <sub>INAC</sub>	F <sub>IN</sub> =AC coupling	0.5		V <sub>DD</sub> -0.5	V	F <sub>IN</sub>
		X <sub>IN</sub> =AC coupling	1.0		V <sub>DD</sub> -0.5	V	X <sub>IN</sub>
Input voltage	V <sub>IH</sub>		V <sub>DD</sub> -0.3		V <sub>DD</sub>	V	RA0 to RA2, DAT, CLK, LE
	V <sub>IL</sub>		0		0.5	V	
Input current 1	I <sub>IH1</sub>	V <sub>IH1</sub> =V <sub>DD</sub>			15	μA	F <sub>IN</sub> , X <sub>IN</sub>
	I <sub>IL1</sub>	V <sub>IL1</sub> =0V			15	μA	
Input current 2	I <sub>IL2</sub>	V <sub>IL2</sub> =0V			30	μA	ENABLE
Input current 3	I <sub>IH3</sub>	V <sub>IH3</sub> =V <sub>DD</sub> T <sub>a</sub> =25°C		0.001	0.1	μA	RA0 to RA2, DAT, CLK
	I <sub>IL3</sub>	V <sub>IL3</sub> =0V T <sub>a</sub> =25°C		0.001	0.1	μA	
Output current PDA, REF <sub>OUT</sub>	I <sub>OH</sub>	V <sub>OH</sub> =V <sub>DD</sub> -0.4V	0.4			μA	øV, øR, PD <sub>P</sub> PDA, REF <sub>OUT</sub>
	I <sub>OL</sub>	V <sub>OL</sub> =0.4V	0.4			μA	
Output leak current	I <sub>LH</sub>	V <sub>LH</sub> =V <sub>DD</sub> T <sub>a</sub> =25°C		0.001	0.1	μA	PD <sub>P</sub> PD <sub>A</sub>
	I <sub>LL</sub>	V <sub>LL</sub> =0V T <sub>a</sub> =25°C		0.001	0.1	μA	
Setup time	DAT → CLK	t <sub>SU1</sub>	300			ns	Fig. 1
	CLK → LE	t <sub>SU2</sub>	300			ns	
Hold time	CLK → DAT	t <sub>H</sub>	300			ns	

■ TIMING CHART

- Input frequency divider data setting



- Input data MSB first.
- Data is input on the rising edge of CLOCK, so it is necessary to change data on the falling edge of CLOCK.
- While the ENABLE signal is "H", data is transferred from the shift register to the input frequency divider's latch. Therefore, ENABLE must go "L" while data is being written into the shift register.

